Product Information

DACOM West

WIZnet

Quick Reference
Hardwired TCP/IP Chips

WIZnet TCP-IP Hardwired Chips integrate additionally to Layers 1 (PHY) and 2 (MAC) also Layers 3 and 4 (TCP/IP) of the Ethernet protocol on gate level. They support TCP, IPv4, UDP, ICMP, ARP, PPPoE and Multicast.

- **2 in 1:** TCP/IP + MAC
- **3 in 1:** TCP/IP + MAC + PHY
- **4 in 1:** Controller + TCP/IP + MAC + PHY

Product List

Parameter / Typ	Integration	Interface				Copper	MDI-X PHY	max. Sockets	Buffer kByte	Temp. Range	Package
		SPI	8 Bit	16Bit/DMA	MII / RMII						
W3150A+	2 in 1	✓	✓		✓	10/100M		4	2x8k	-40°...85°C	64-LQFP
W5100	3 in 1	✓	✓			10/100M	✓	4	2x8k	-40°...85°C	80-LQFP
W5500	3 in 1	✓				10/100M	✓*	8	32k	-40°...85°C	48-LQFP
W5300	3 in 1		✓	✓	✓	10/100M	✓	8	128k	-40°...85°C	100-LQFP
		RAM	Flash	Controller	ext. I/F						
W7500 W7500P	4 in 1	16-48k	128k	Cortex-M0	13/48 GPIO	10/100M	- ✓	8	32k	-40°...85°C	64-TQFP
W7100A	4 in 1	64k	64k	8051	32 GPIO 19 GPIO	10/100M	✓	8	32k	-40°...85°C	100-LQFP 64-QFN

* non MDI-X PHY

General Features

- Hardwired TCP/IP:
  - TCP, UDP, ICMP, IGMP, IPv4, ARP, Ethernet
  - 4 or 8 independent sockets simultaneously
  - Supports hybrid TCP/IP stack for software protocols
  - Internal Dual-Port-RAM (TX/RX buffer 16-128kB)
- Embedded Ethernet-MAC:
  - IEEE 802.3 (10Base-T) and 802.3u (100Base-TX)
  - Multicast
  - Connection PPPoE protocol with PAP/CHAP authentication mode for ADSL
- Interface:
  - 8/16 Bit Address/Data Bus for direct- & indirect-mode and DMA
  - SPI-mode 0 and 3
- between 3 Mbit/s and 80 MBit/s throughput at application layer
- LED outputs: full-/half-duplex, link, speed
- 3.3V operation with 5V I/O signal tolerance

W7500 Special Features:

- ARM Cortex-M0 Core, 50MHz
- 4 timers / 8 PWMs, watchdog and RTC
- 3 UART, 2 SPI, 2 I²C Interfaces
- 1 Random Number Generator (32-bit)
- 48 I/Os (G PIO 0, 1, 2, 3)
- TQFP-64 Package (7x7mm)
- W7500P with integrated IC+ IP101G PHY

W5500 Special Features:

- Power Down mode: 13mA typical
- Wake on LAN
- Very stable integrated non MDI-X PHY
- Fast SPI Interface (80 MHz)
- 48-LQFP Package 7x7mm, 0.5mm pitch

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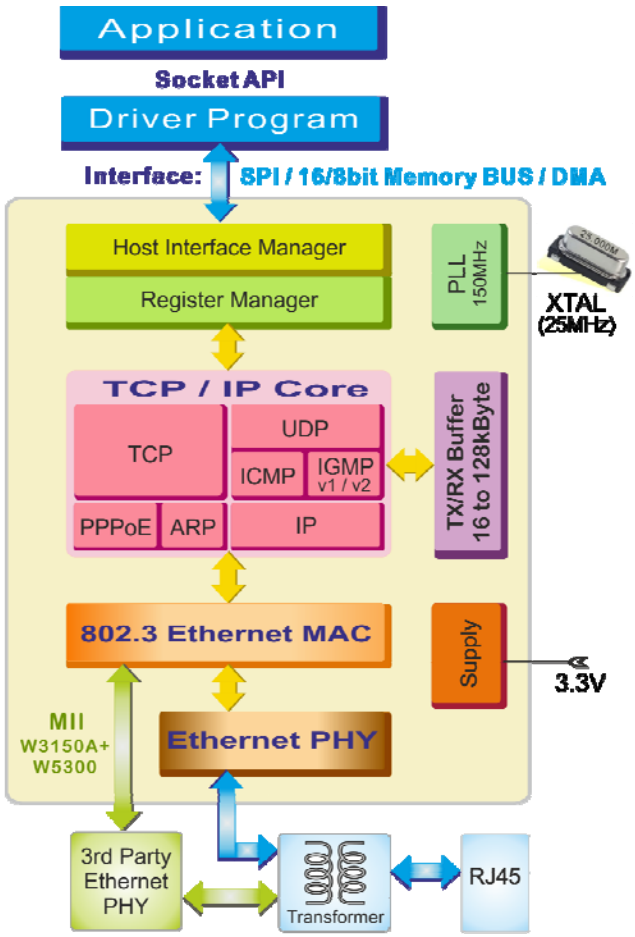
Block Diagram Hardwired TCP/IP



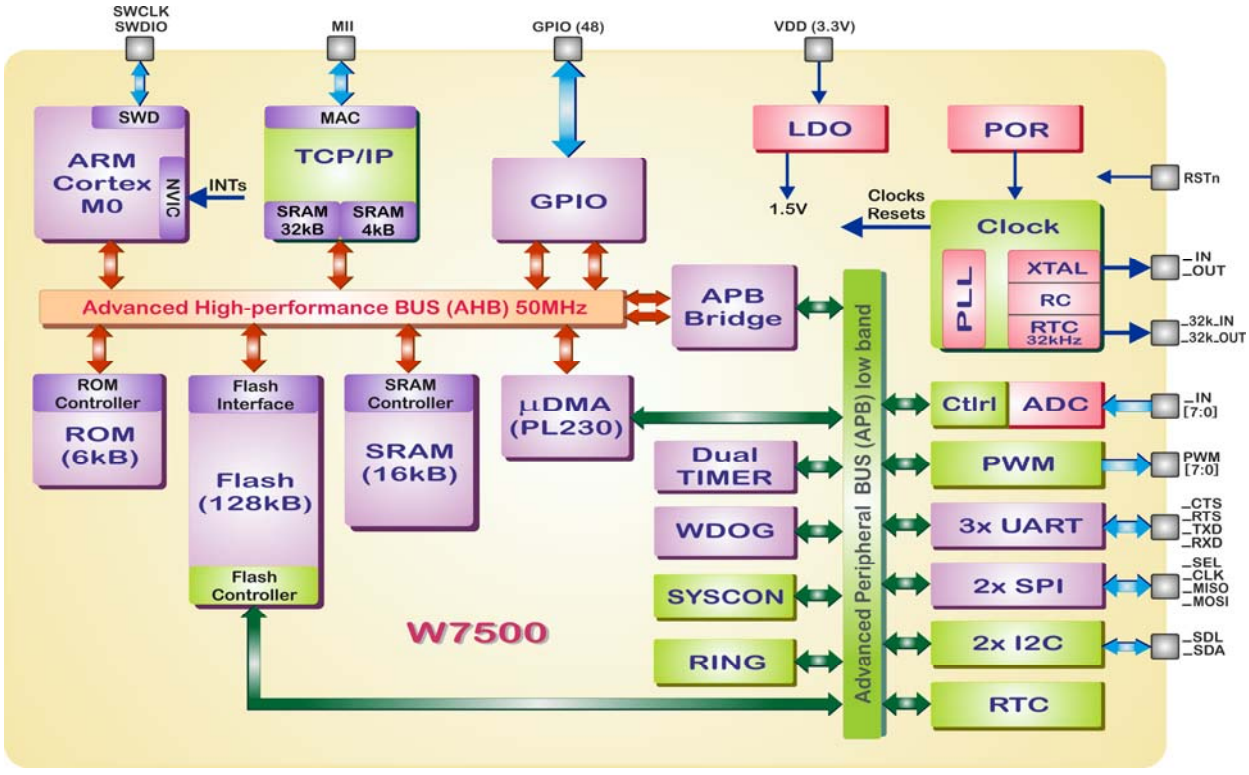
WIZ820io Module

- Board size:
  23 x 25mm^2
- Interface Connector:
  two 6 pin headers 2.54mm pitch

Applications

- Home Network & Set-Top Boxes
- Serial-to-Ethernet - Gateways
- Smart Metering
- GPIO-to-Ethernet - Sensor Network
- Security Systems & Cameras
- Factory and Building Automation
- Medical Monitoring Equipment
- Embedded Server

Block Diagram W7500



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