PCB Module

Design Guide

Application Note

AN-PCB1-01

Version: 0.0
Released Date: 2007/9/12

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PCB Module
Design Guide

1. Purpose

The purpose of this guide is to provide UBEC's customers some practical guidelines and tips for a good module printed circuit board (PCB) layout and implementation.

2. Check Items

A sound module PCB layout must take into consideration certain not so obvious yet critical items. If these items were not included in the board layout design, the performance of the realized board may not meet its designed goals. These items listed as below are for the designer's reference. It must be emphasized, however, that following these good practices is just the necessary conditions to ensure good RF performance. A good general basic board design is still a must.

(1) Verify that the board parameters such as the copper clad layer thickness, the dielectric constant, the total board thickness, transmission line width, plated gold thickness etc. are such that the resultant characteristic impedance of the transmission lines would be 50 Ohms.

(2) Make sure that the grounding layers of the transmission lines are continuous and not cut through by other circuits.

(3) The top and the bottom of the grounding layers as well as the grounding via-holes of the integrated circuit (IC) must not be covered with any insulating paint. Their areas must be large enough and exposed for the wetting area. The minimum inner diameter of the via-holes must be greater than 0.3mm and the via-holes have to have sufficient solder zones.

(4) Avoid placing circuit components and/or circuit routing on the top or bottom layers directly above or below where a power amplifier is situated.

(5) Do not place metal surfaces or metallic components directly below the areas where the antenna is located to ensure that the operation of the antenna is not compromised.

(6) Leave adequate spaces surrounding a power amplifier whose output power exceeds 10 mW. This is to allow for installing shielding devices later should they become needed.

3. RF Transmission Line Characteristic Impedance

In order to achieve the most efficient RF energy transmission along transmission lines, the best approach is to use transmission lines with the same characteristic impedance throughout the circuit. The 50 Ohm line impedance has been widely used in the RF design for such a long time that it has essentially become the defector standard.
For the module PCB, there are two commonly used transmission lines. One is the microstrip, while the other is the co-planar waveguide as illustrated in Figures 1 to 4.

3.1. Design for a Microstrip

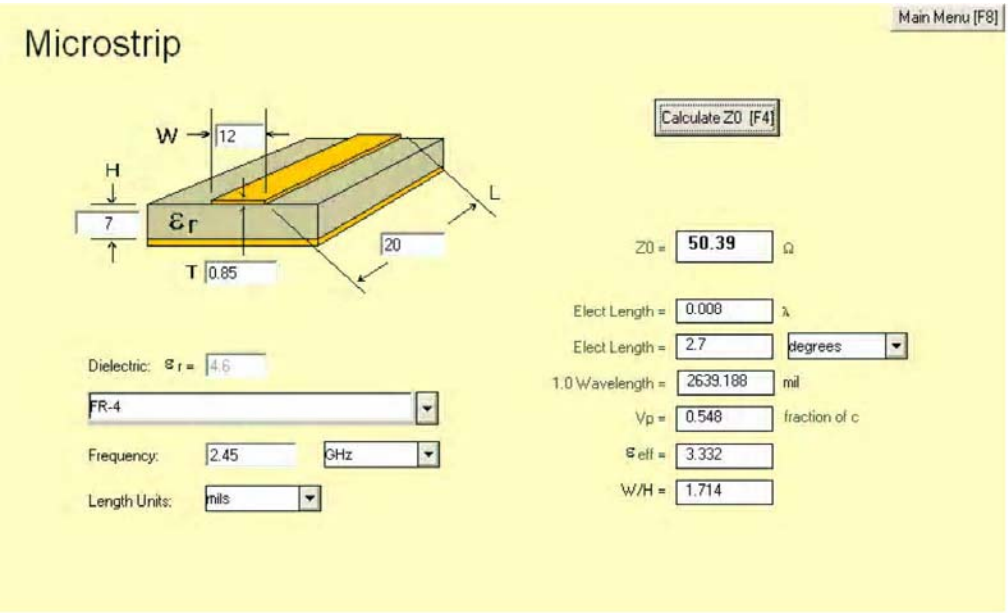


Figure 1. Example for the Design of a Microstrip Line

3.2 Calculation of Characteristic Impedance for a Microstrip

To calculate the characteristic impedance (Z), inputting the microstrip line width (W), the dielectric thickness (H), signal line metal thickness (T), and the dielectric constant (ε) into the following set of equations (also refer to http://www.emclab.umr.edu/pcbtlc).

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) \quad \textbf{ohms}$$

$$t_{pd} = 1.016\sqrt{0.475\,\varepsilon_r + 0.67} \quad \textbf{ns/ft}$$

$$0.1 < \frac{W}{H} < 3.0, \quad 1 < \varepsilon_r < 15$$

t_{pd}: the propagation delay per unit

Impedance Matching: Normally the input or the output impedance of an antenna, a transmitter, or a receiver is designed to be 50 Ohms. To achieve the most efficient power transmission, the inter-component transmission lines must also be designed for 50 Ohms.

3.3 General Microstrip Design Recommendations

(1) The length of the microstrip line should be kept as short as possible. Lengths over 2.54 cm (1 inch) should be avoided as much as possible for the standard PCB materials and for designs without the additional shielding.
(2) The distance between a microstrip line and the top layer ground should be made at least as large as the dielectric thickness. Otherwise the propagating characteristics of a microstrip will be degraded.
(3) All of the micro-strip line designs should follow the 50Ω impedance design rule to avoid any transmission loss and achieve the best performance. (please refer to Figures 2 to 5)
(4) When routing a microstrip line from the chip output port to the antenna, one should follow the following design rules: the whole length of the microstrip line should have a common continuous grounding plane. (Please refer to Figure 6.)
(5) Avoid routing the RF path too close to the digital circuitry.
(6) To reduce the effects from the signal reflection, sharp angles (or turns) in the routing of the microstrip line should be avoided. Chamfers or fillets are preferred. If achievable, a 45-degree turn is always preferred over a 90-degree one.
(7) Avoid routing the RF signal underneath a RF chip or a RF power amplifier.

3.4 Examples of Co-Planar Waveguide Design

Strictly speaking, the ground planes for a co-planar waveguide lie on the two sides of the signal line on the same surface. There is no additional ground plane lying below the signal line. In reality, the co-planar waveguides are often implemented in a multi-metal layer structure shown as the Figure 2. In this configuration, one or more of the metal layers may be used as a grounding plane, resulting in a situation where an additional ground plane is present below the signal line. The propagation mode for this "hybrid" transmission line is a mixture of the microstrip and a pure co-planar waveguide. If the effect due to the presence of the ground plane below the signal line is very small, the hybrid transmission line will essentially act like a pure co-planar waveguide. However, when using the common multi-layer board, one find that the effect from the presence of the additional ground plane below the signal line cannot be neglected as illustrated in examples shown as below where the line impedance for two configurations are calculated and compared. (Figures 3 and 4)

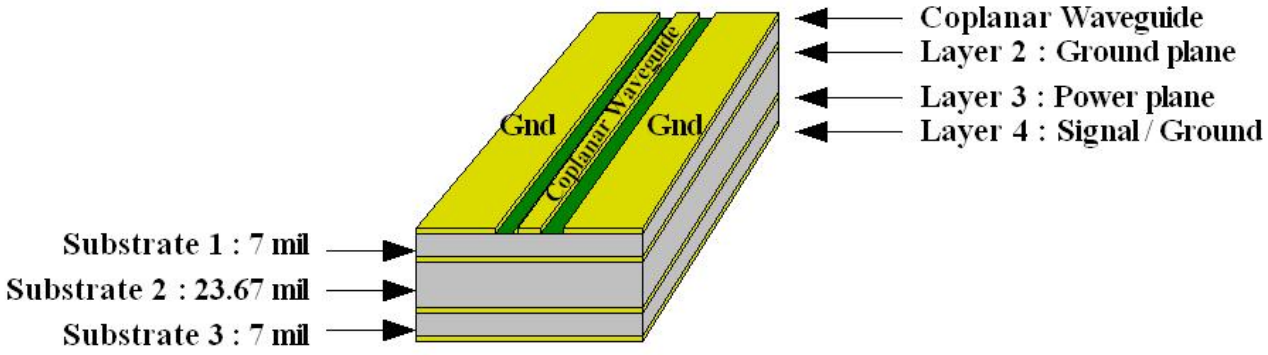


Figure 2. Board Structure of the Typical Four-Layers

Copper Toper Layer = 0.85 mils (0.5 oz，0.15 mils gild)
Substrate 1 = 7 mils
Copper Midlayer1 = 0.7 mils (0.5 oz)
Substrate 2 = 22.27 mils
Copper Midlayer2 = 0.7 mils (0.5 oz)
Substrate 3 = 7 mils
Copper Bottom Layer = 0.85 mils (0.5 oz， 0.15 mils gild)
Total = 39.37 mils (1.0 mm)

Design of a Co-Planar Waveguide

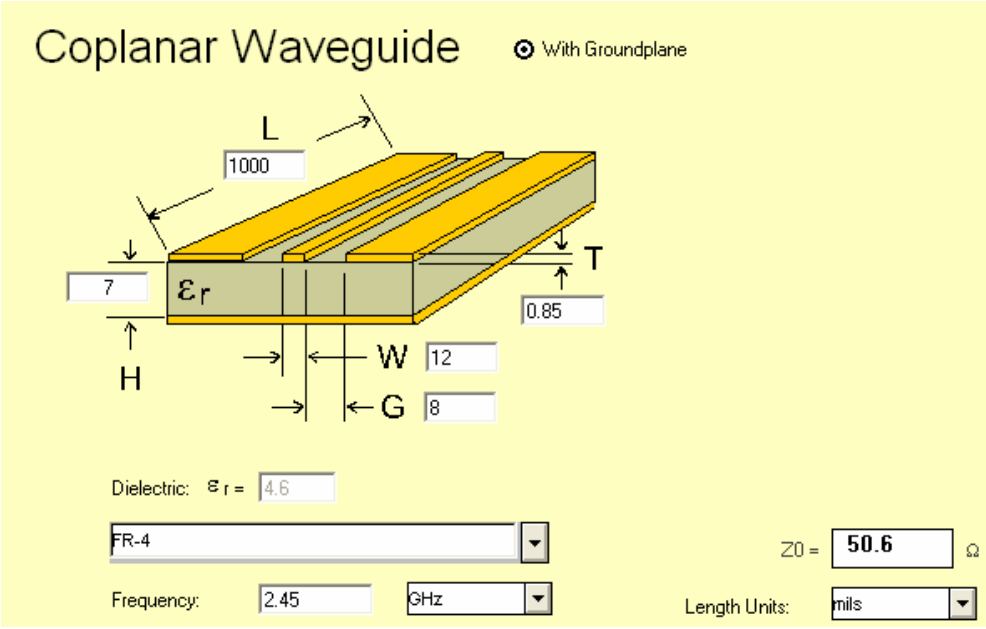


Figure 3. Example of the Co-Planar Waveguide Design

If the dielectric constant is 4.6(FR4), to obtain a line impedance of the 50 Ohms require the signal line width to be 12 mils and the signal line-ground plane gap 8 mils using the commercial design software.

- (W) = 12 mils
- (G) = 8 mils
- Because the UBEC's module is quite small, using Figure 3 example is more appropriate.

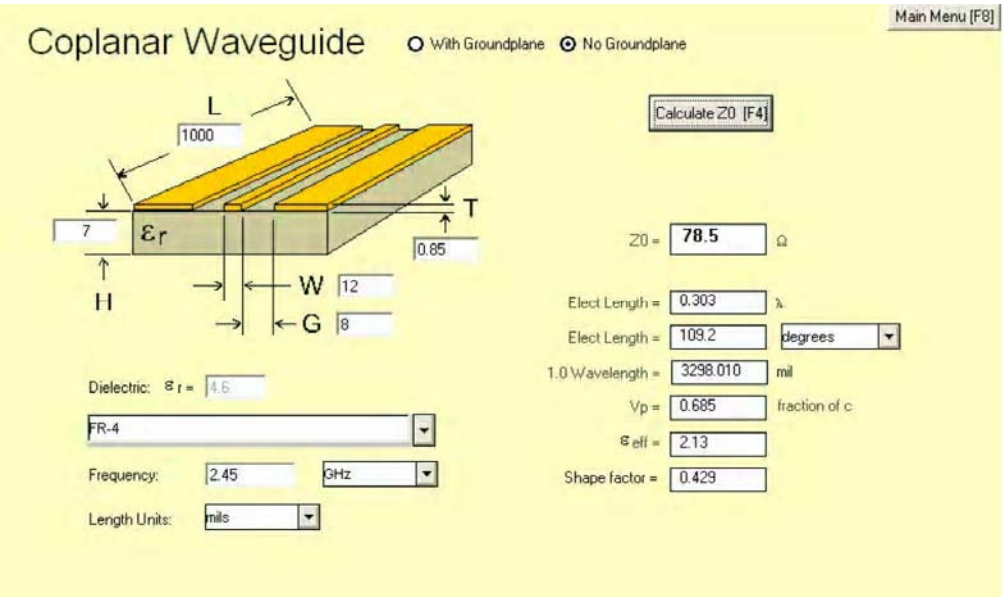


Figure 4. Co-Planar Waveguide Design Example

Figure 4 is an example of a pure Co-Planar Waveguide. If we use the same signal line width and the signal line-ground plan gap, the calculation shows that a characteristic impedance of 78.5 (instead of 50) Ohms is obtained. This example demonstrated that the effect from the additional ground plane is not negligible.

3.4 General Co-Planar Waveguide Design Recommendations

Other than the item #3 listed in Section 3.2, all the recommendations for the microstrip design are equally applicable to the Co-Planar Waveguide design.

4. RF Grounding and Ground Via-Hole

4.1 Grounding

Achieving a good grounding is very critical for RF circuit designs. Poor grounding not only degrades the circuit performance, but also reduces the production yield; it can also result in undesirable effects (such as circuit oscillation). UBEC provide a few tips for achieving a good RF grounding.
Separate out the digital and the RF/Analog circuit areas so that each has its own routing and grounding areas.

Also it is recommended to separate out areas where high current or high temperature operation would occur. When using a 4-layer board, one can use one of the layers (e.g. layer #2) as a grounding layer to screen out the RF signal interference upon other circuitry residing on other layers.
Minimize the path length from the circuit to the ground so as to reduce the stray pick-up and the possibility of the electro-magnetic interference (EMI).

4.2 Ground via-hole

A ground via-hole provides a convenient and the shortest path length to electrically and vertically connecting different metal layers for an IC. However, at high frequencies, such via-holes present an inductive effect to the circuit performance. For example, for a 1.6 mm thick 4-layer board, if a 0.2 mm diameter via-hole is drilled from the top layer to the second layer (ground layer), such a via-hole will have 0.75 nH inductance. At the 2.5 GHz commonly used ISM (Industrial, Scientific, and Medical) band, this inductance will result in a 12 Ohm reactance, and there will be a RF potential difference between the top and the second layer and the top layer is not really a true ground. Therefore, it is important to minimize its inductance for the via-hole design.

For a good board design, one can use many via-holes for the grounding purpose. The advantages are several: one can reduce the effective inductance due to the parallel effect of the multiple inductors, and one can avoid a single-point failure. The latter consideration is especially critical for QFN (Quad Flat No-lead) Package where a poor design or soldering can result in degraded amplifier noise figure. For a power amplifier, the configuration of the multi via-holes has the beneficial effect of improved heat dissipation due to multiple heat paths.

5. Correct Examples

5.1 Applicable Package Type

QFN 7*7
QFN 6*6
QFN 5*5
QFN 3*3
QFN 2*2
VQFN 3*3

5.2 Approach

The via-holes and the grounding areas should not be covered with any anti-solder paint. Sample #1 and the sample 2 (Figure 5 to Figure 8) illustrate that within the red squares, the top and the bottom layers of the via-holes are not covered with anti-solder paint.

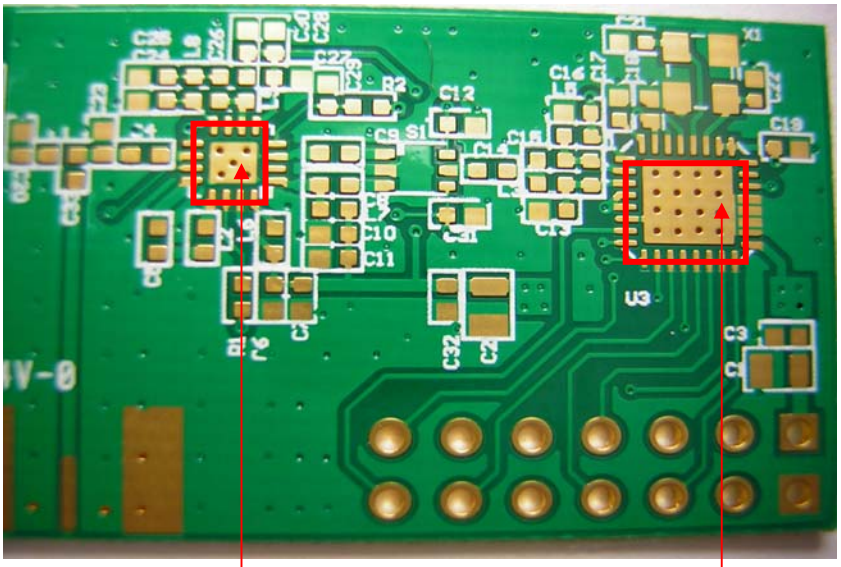


Figure 5. Top Side of Sample #1

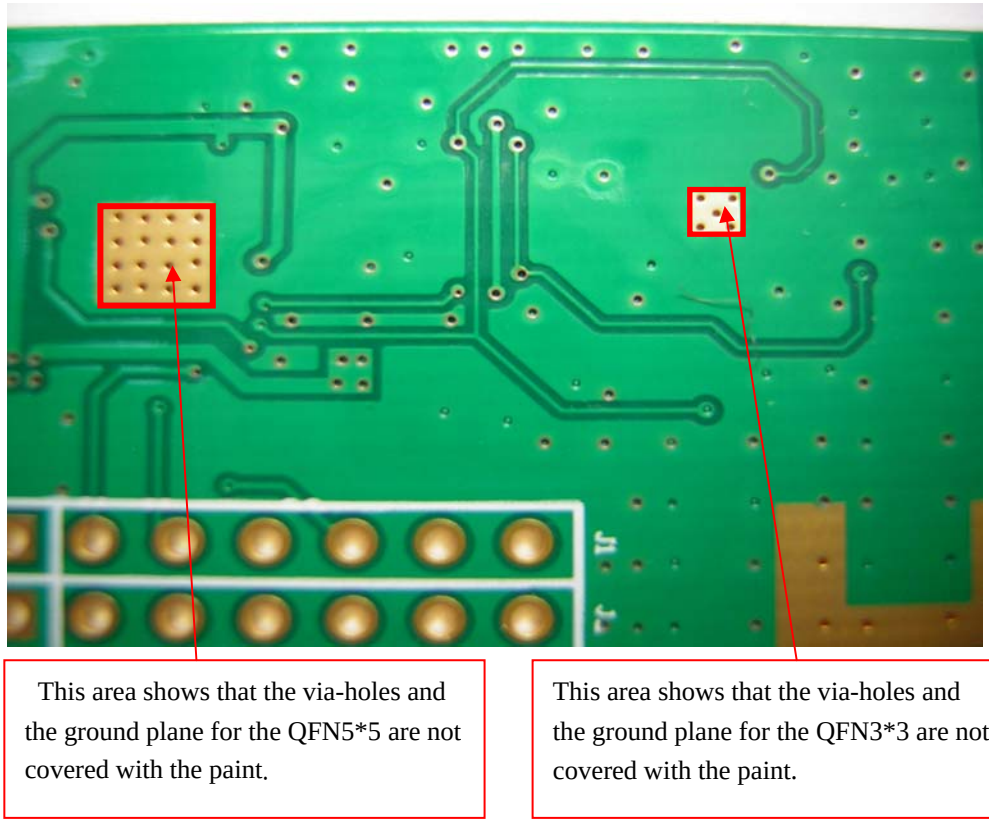


Figure 6. Bottom Side of Sample #1

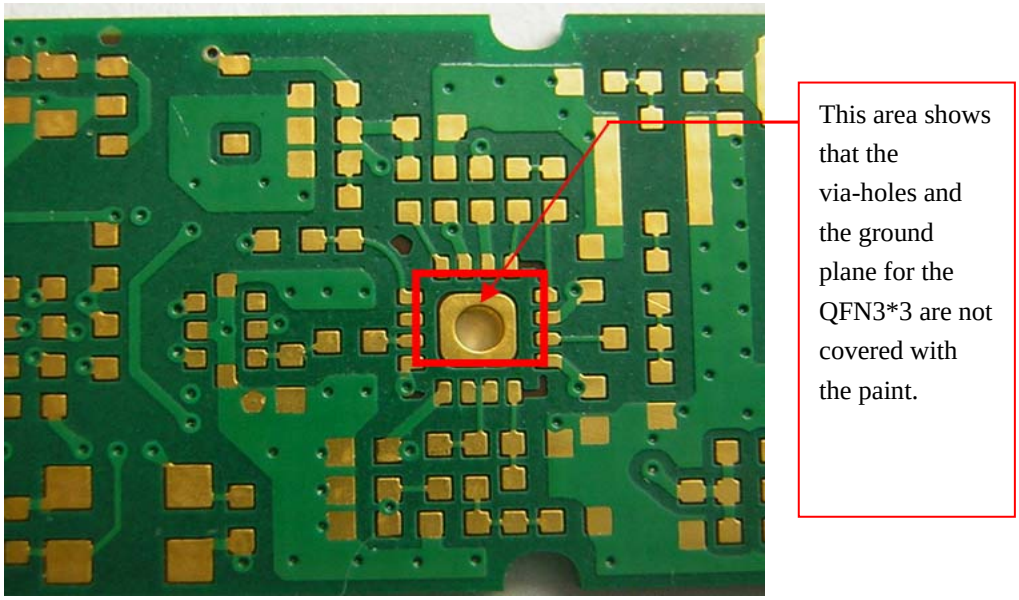


Figure 7. Top Side of Sample # 2

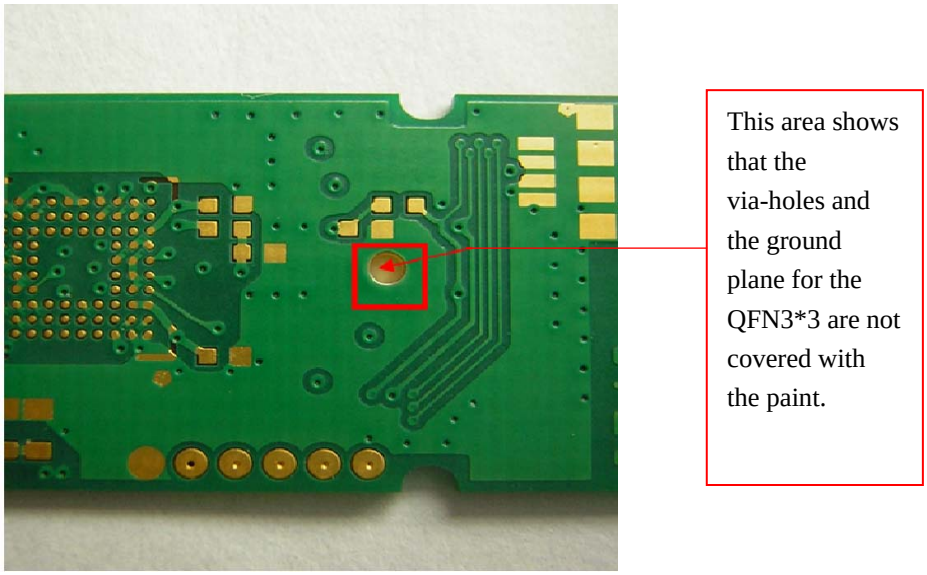


Figure 8. Bottom Side of Sample #2

5.3 Suggested approach for SMT (Surface Mount Technology)

For the SMT soldering process, to avoid poor solder contact due to the cold soldering or uneven bulging surface, it is recommended that not more than 40% of the ground plane surface be coated with solder paste and the hot pad area should not occupy more than 50~60% of the grounding plane area.

The following is a stencil drilling hole dimensions for QFN 2x2 package.

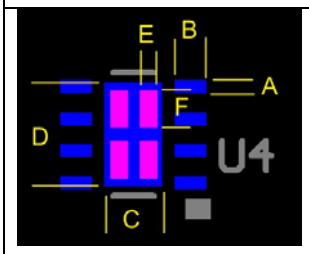
UP2202 SMT Stencil Drill Dimension (Thickness=0.13mm)		
	PCB PAD Original Dimension	Stencil Drilling Hole Dimension
	A: 7.9mil B: 19.3mil C(ground): 35.4mil D(ground): 63mil	A: 8.6mil B: 25.3mil E(ground): 10.8mil F(ground): 23mil (E * F) * 4ea = approximately occupying 44.5% of the IC grounding area

Figure 9. The Ground Area and the Solder Paste Dimension for QFN 2x2 Package

6. Incorrect Examples

The following examples all show that the via-holes and the grounding areas are covered with anti-solder paints.

Both figures 10 and 11 are faulty examples. The red lined area shows top/bottom of via-holes with solder mask ◦ × means a fault and the corrective action is given in the rectangular frame

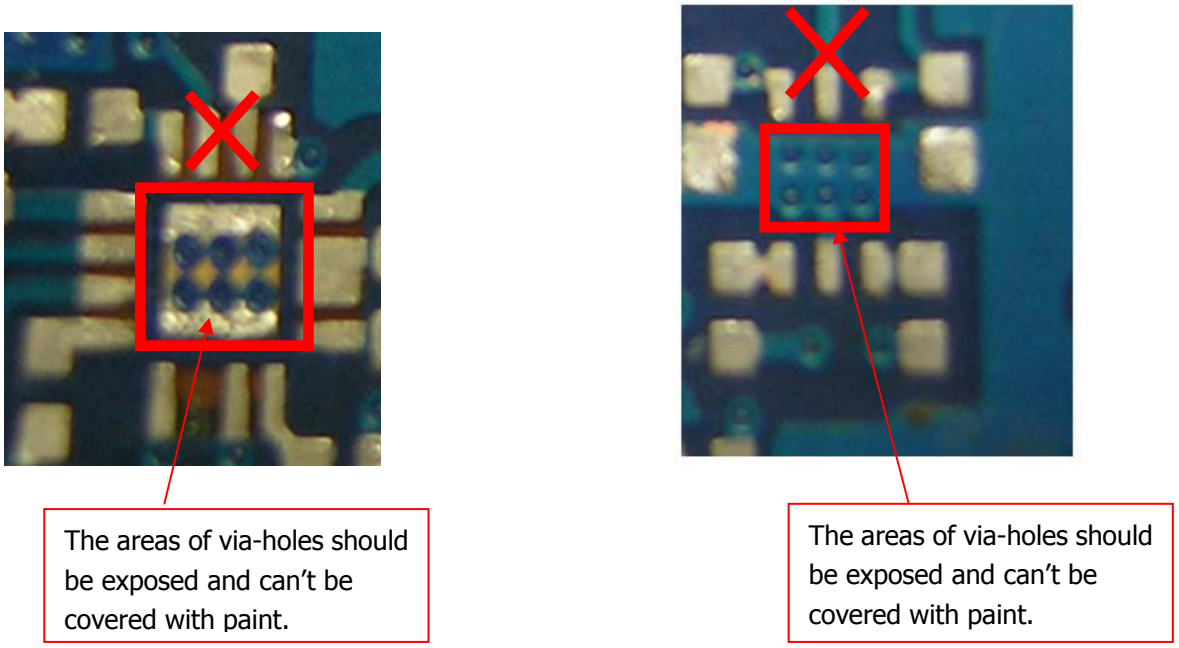


Figure 10. Top Layer (left) and Bottom Layer (right)

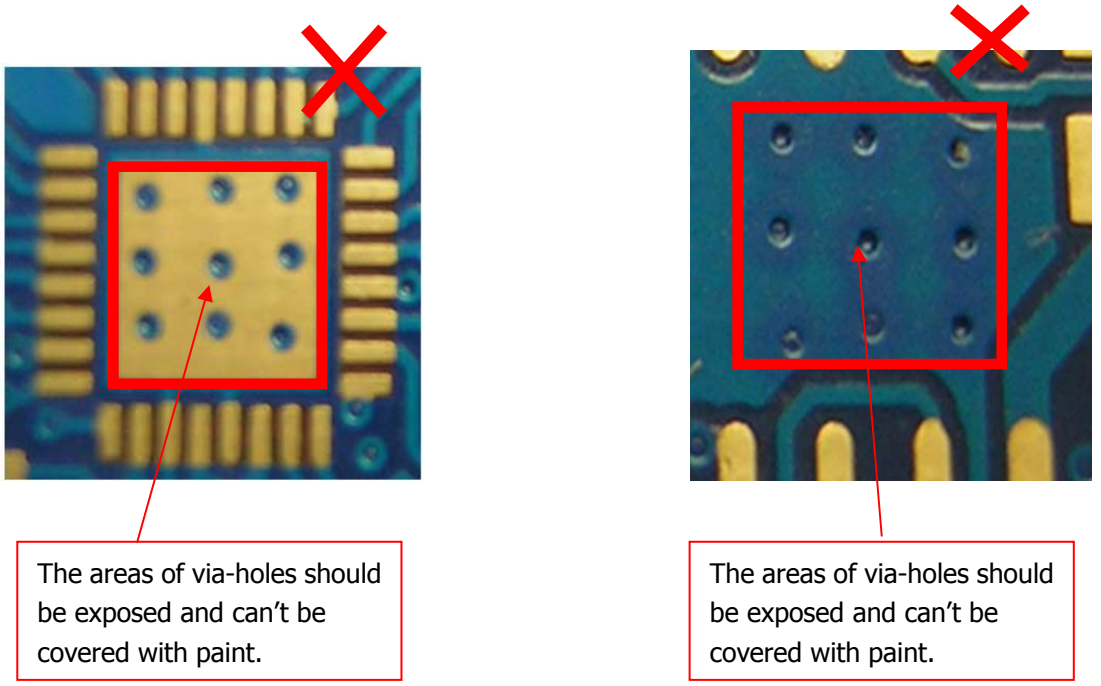


Figure11 . Top Layer (left) and Bottom Layer (right)

Revision History

Revision	Date	Description of Change
0.0	2007/09/12	Initial version

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