US2400-EVB

Low Power 2.4GHz Transceiver
for
IEEE 802.15.4 Standard

Revision History Hardware

Revision	Date	Description of Changes
V01 / V02	Sep. 2011	Initial release
V03	Dec 2011	Addition 4.1 Evaluation Board Variants and 5.3 Connector Interface J1

Table of Contents

1. Introduction

The US2400 IC is a solution that complies with IEEE 802.15.4-2006 specifications. It integrates a 2.4 GHz RF-transceiver with an IEEE802.15.4 compliant Baseband/MAC block within a single chip. The US2400 can be controlled by a microprocessor (e.g. 8051) for low-data-rate applications such as home automation, industrial automation, consumer electronics, PC peripheral …etc. For medium-data-rate applications like wireless voice and image transmission, the US2400 provides 1M/2M bps turbo mode.

The RF block of the US2400 integrates receiver, transmitter, voltage-controlled oscillator (VCO), and phase-locked loop (PLL). It uses advanced radio architecture to minimize the external component count and the power consumption. The Baseband/MAC block provides the hardware architecture for both IEEE 802.15.4 compliant MAC and PHY layers. It mainly consists of TX/RX control, CSMA-CA controller, "Superframe" constructor, security engine and digital signal processing module.

1.1 Key Features US2400

RF / Analog

- ISM band 2.405 ~ 2.480 GHz operation
- IEEE 802.15.4-2006 specification compliance
- RF sensitivity: -94 dBm @ 250kbps
- Maximum RF input level: 3dBm
- RSSI range: 44dB @ 250kbps
- RF output power: 1 dBm typical
- RF output power control range: 40 dB
- Single End RF input/output
- 1M/2M bps turbo mode supported
- Current consumption in RX Mode: 20.4mA
- Current consumption in TX Mode: 25.5mA
- Idle Mode: 6mA/ Halt mode: 1.8mA
- Standby mode: 5.1 µA/ Deep sleep mode 4µA
- Power down mode: 0.1µA
- 32 MHz reference clock output
- Digital VCO and filter calibration
- Integrated RSSI ADC and I/Q DACs
- Small 24-pin leadless LGA 6x6 mm^2 package
- Few external component count

MAC / Baseband

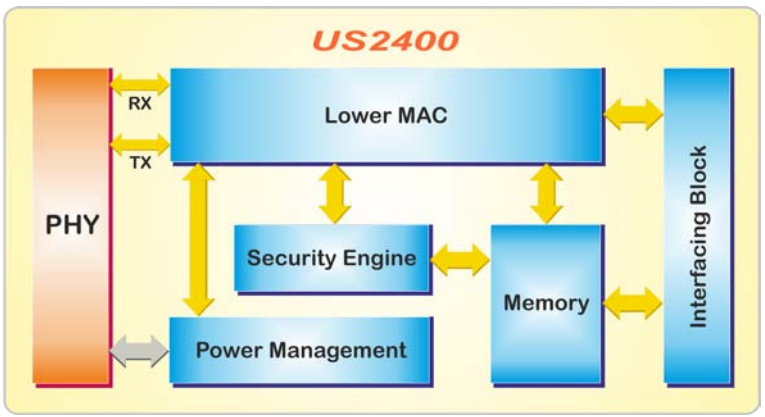
- IEEE 802.15.4-2006 specification compliance
- Hardware CSMA-CA mechanism, automatic ACK response and FCS check
- Programmable "Superframe" construction
- Functionally independent TX FIFOs, including beacon FIFO, transmit FIFO and GTS FIFOs
- Dual RX FIFOs
- Hardware security engine (AES-128)
- Various power saving modes
- Support all CCA modes and RSSI/LQI
- Simple 4-wire SPI interface

2. Functional Description

2.1 US2400 Chip Block Diagram

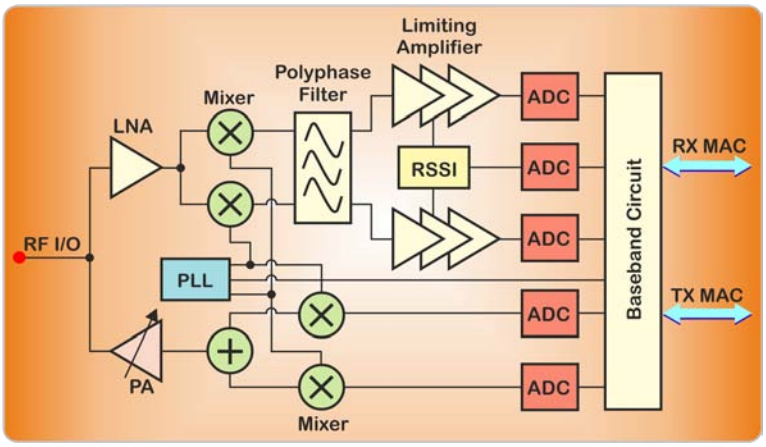
The UZ2400 is composed of the following six blocks:

- PHY block
- Lower MAC block
- Memory block
- Power management block
- Security block
- Interfacing block



2.2 PHY Block Architecture

The PHY (physical) block is compliant to IEEE 802.15.4-2006 2.4GHz ISM band standard.



2.2.1 IEE 802.15.4-206 PHY Introduction

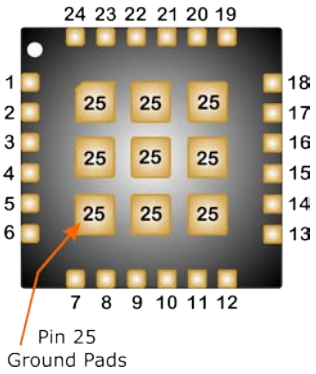
Although a brief introduction of IEEE 802.15.4-2006 PHY layer is available in datasheet US2400, it is recommended that user should read the specification of IEEE 802.15.4-2006 for more comprehensive understanding.
The UZ2400 provides a transceiver which is fully compatible to IEEE 802.15.4-2006 2.4GHz band PHY layer specifications.

For more detailed information, please refer to the latest US2400 data sheet revision

3. Device Pin Description

Pin	Pin Name	I/O Type	Description
1	RESETn	Input	Global hardware reset pin, active low
2	WAKE	Input	External wake up trigger
3	INT	Output	Interrupt pin to microprocessor
4	SO	Output	Serial interface data output
5	SI	Input	Serial interface data input
6	SCLK	Input	Serial interface clock
7	SEN	Input	Serial interface enable
8	VDD	power	Power supply (3V)
9	RF_IN2	Output	reference clock output
10	XTAL_N	Input	32 MHz Crystal input (−)
11	GND	Ground	Ground
12	XTAL_P	Input	32 MHz Crystal input (+)
13-15	GND	Ground	Ground
16	RF	Analog I/O	RF input / output
17-18	GND	Ground	Ground
19-21	GND	Ground	Ground
22	GPI0	Digital I/O	General purpose digital I/O; also used as an external PA enable
23	GPI1	Digital I/O	General purpose digital I/O; also used as an external TX/RX switch control
24	GPI2	Digital I/O	General purpose digital I/O, also used as an external TX/RX switch control
25	GND	Ground	Ground / bottom side

Top view



4. Application Guide

Some typical applications are described in this chapter to help a user gain more understanding of the operation of the US2400.

A typical connection using the SPI interface is shown as below. The MCU host serves as a master role, and the US2400 serves as a slave role. The values of C1, C2 and C3 are decided by Antenna.

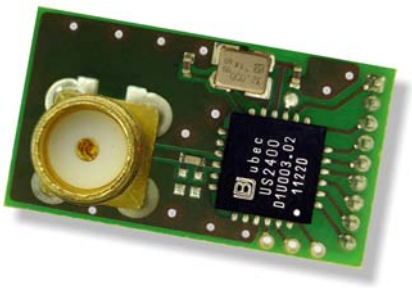
The US2400 registers and FIFOs can be accessed by the SPI interfaces. They are categorized into two kinds of address spaces. One is the short address space; the other is the long address space.

⇨ See data sheet US2400 to "Registers and FIFOs".

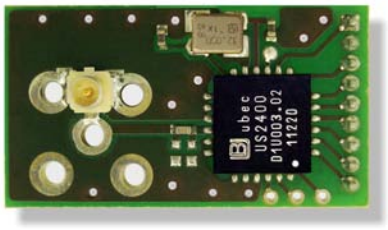
4.1 Evaluation Board Variants

Type	Board Execution		Part No.
US2400-	CS	Connector version SMA	US2400-CS
	CU	Connector version U.FL	US2400-CU
	A	Antenna version	US2400-A

50Ω Connector Board Variant SMA

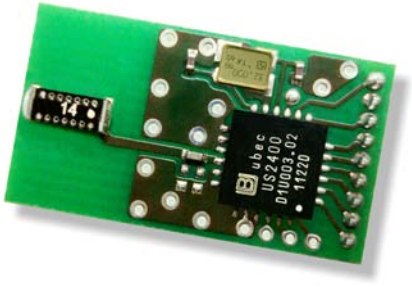


US2400-CS



50Ω Connector Board Variant U.FL

US2400-CU

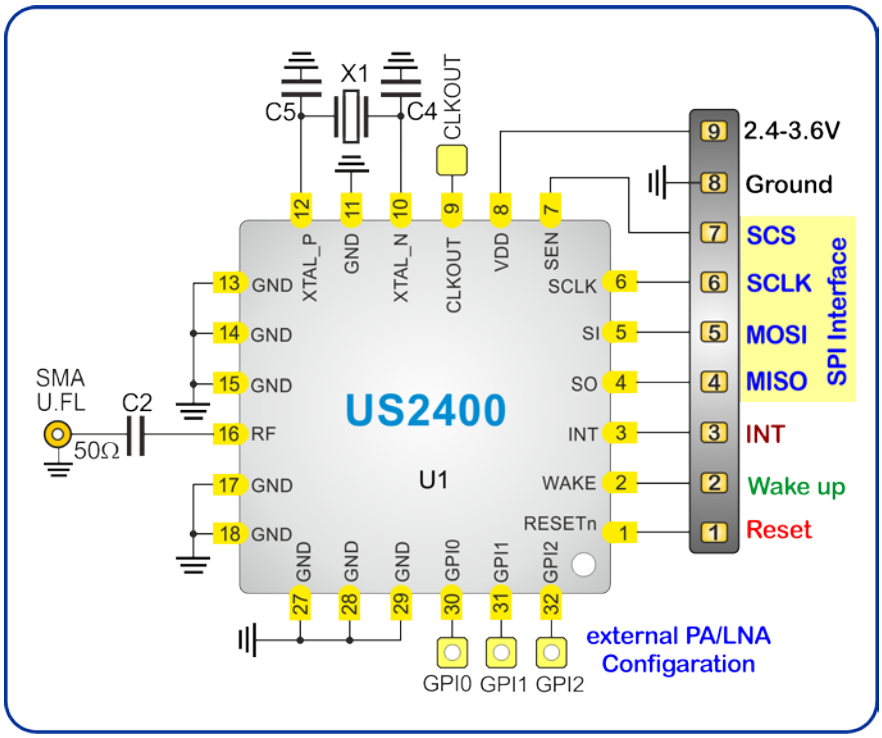


Antenna Board *(Chip Antenna)*

US2400-A

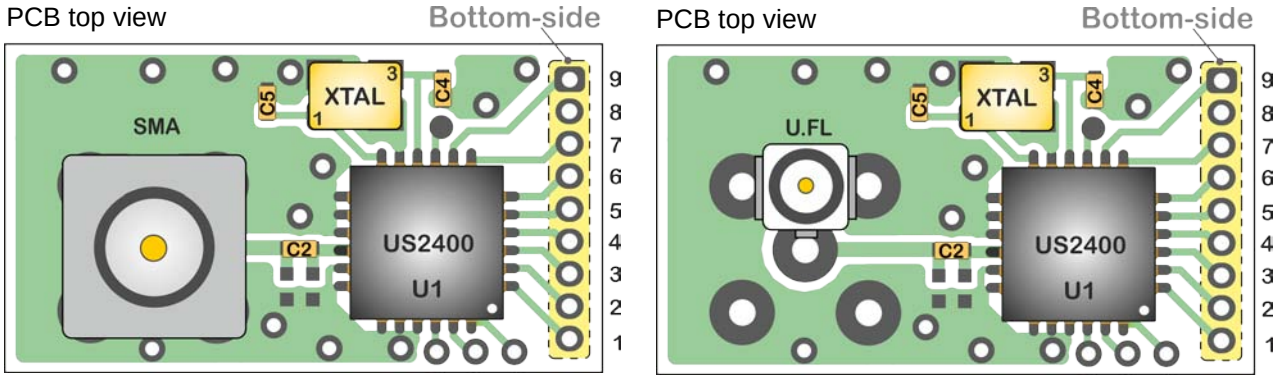
5. Evaluation Board Variants

5.1 50Ω Connector Board (US2400-C) Circuit Diagram

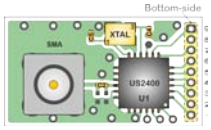


5.1.1 Component Arrangement 50Ω Connector Board for SMA & U.FL

on a scale of 3:1



Board size: 23.7mm(X) / 13.2mm(Y)



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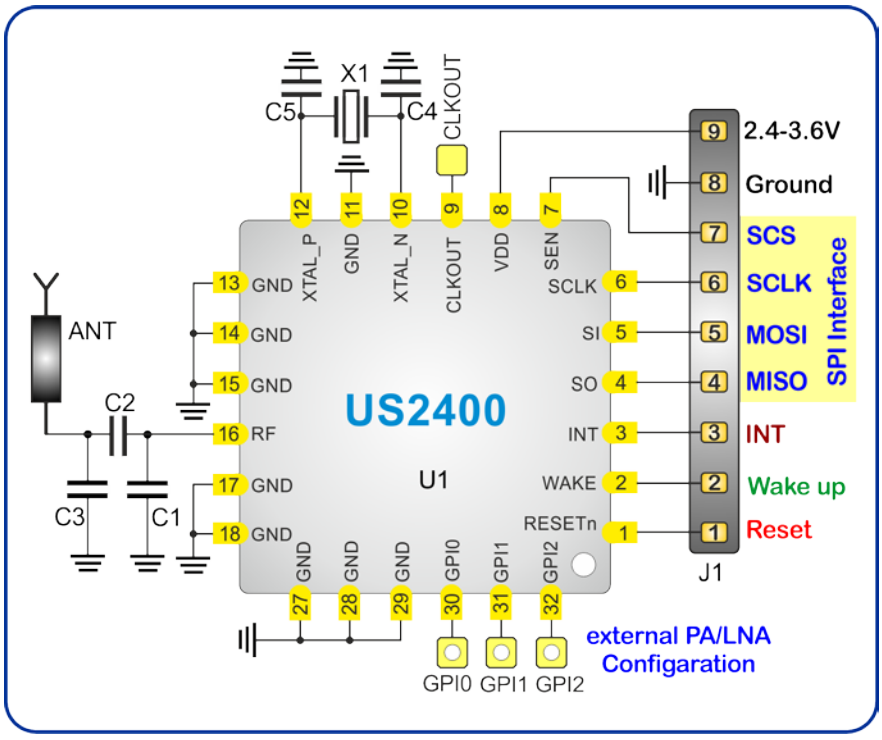
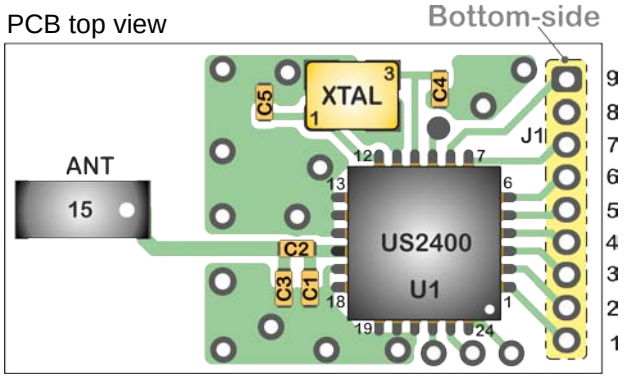
5.2 Antenna Board (US2400-A) Circuit Diagram

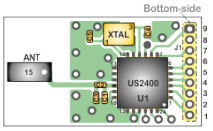


5.2.1 Component Arrangement Antenna Board (Chip Antenna)

on a scale of 3:1



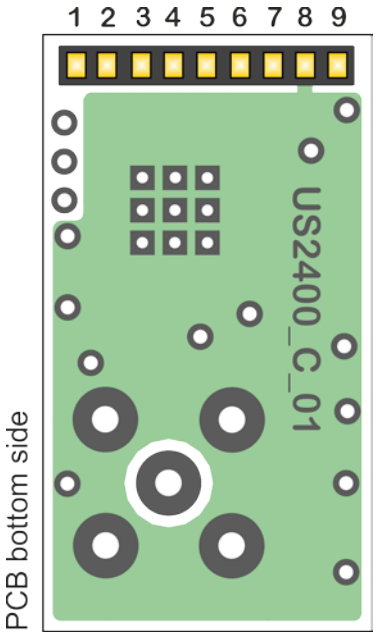
Board size: 23.7mm(X) / 13.2mm(Y)



on a scale of 1:1

5.3 Connector Interface J1 (SPI Communication)

Pin	Pin Name	Description
1	RESETn	Global hardware reset pin, active low
2	Wake up	External wake up trigger
3	INT	Interrupt pin to microprocessor
4	MISO	Serial interface data output
5	MOSI	Serial interface data input
6	SCLK	Serial interface clock
7	SCL	Serial interface enable
8	GND	Ground
9	VDD	Power supply 2.4 - 3.6V



5.4 Board Component Values to 5.1 and 5.2

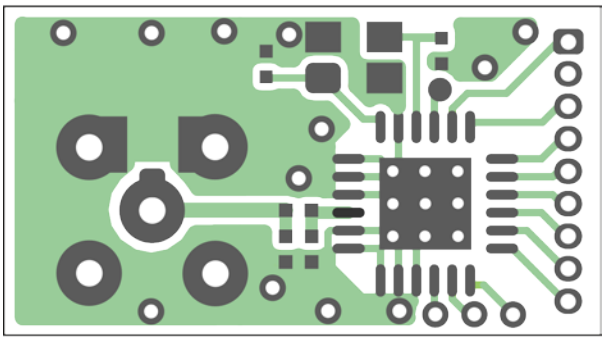
Part	Size	Value	Toler.	Description
U1	LGA 6x6	US2400		2.4 GHZ Transceiver
C1	0402		±5%	Capacitor to match antenna, optional
C2	0402	2.2 pF	±5%	Capacitor
C3	0402		±5%	Capacitor to match antenna, optional
C4	0402	8.2 pF	±5%	Capacitor for NX3225SA-STD-CSR-6/-3
C5	0402	8.2 pF	±5%	Capacitor for NX3225SA-STD-CSR-6/-3
X1	SMD 2.5 x 3.2 x 0.55 mm	32.000MHz	±10ppm cal. ±10ppm temp.	fundamental-mode crystal: NX3225SA-STD-CSR-3 from NDK CL=8pF, -10 to 75°C or equivalent part
		32.000MHz	±15ppm cal. ±25ppm temp.	fundamental-mode crystal: NX3225SA-STD-CSR-6 from NDK CL=8pF, -40 to 85°C or equivalent part
ANT	5 x 2 x 1 mm	PCAK0000-15		2.4 - 2.5 GHz from Cirocomm Technology Part Nr.: 03C15D4Y0000510
SMA	SMA	50Ω		Connector optional
U.FL	U.FL	50Ω		Connector optional
J1		9 pin		Connector, 1.27 pitch

6. PCB Layouts

6.1 50Ω Connector Board Layout

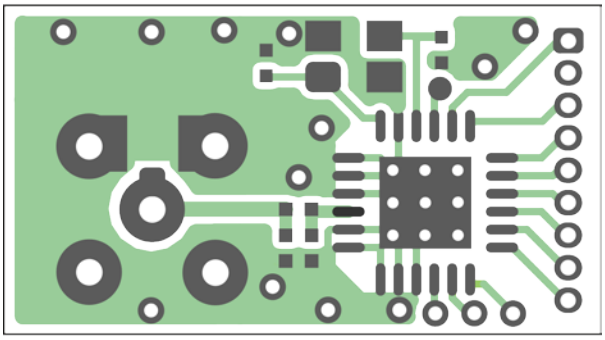
on a scale of 3:1

PCB top view



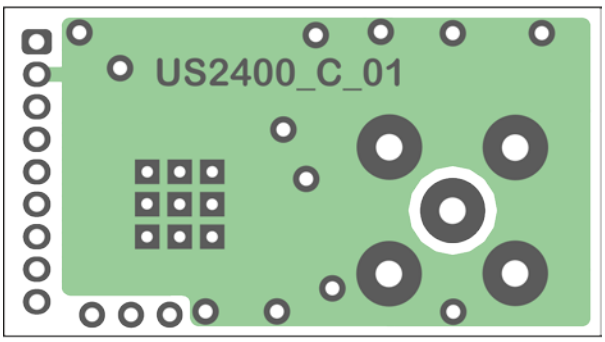
Board size: 23.7mm(X) / 13.2mm(Y)

PCB top view



Board size: 23.7mm(X) / 13.2mm(Y)

PCB bottom side

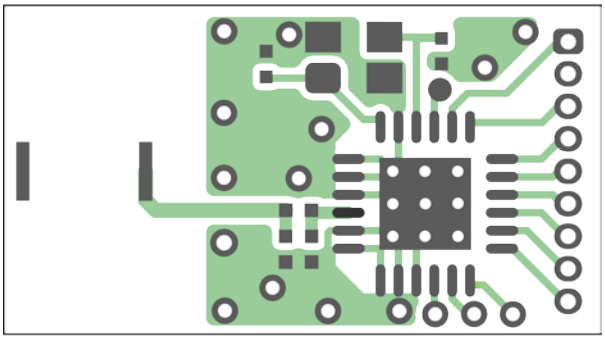


Board size: 23.7mm(X) / 13.2mm(Y)

6.2 Antenna Board Layout

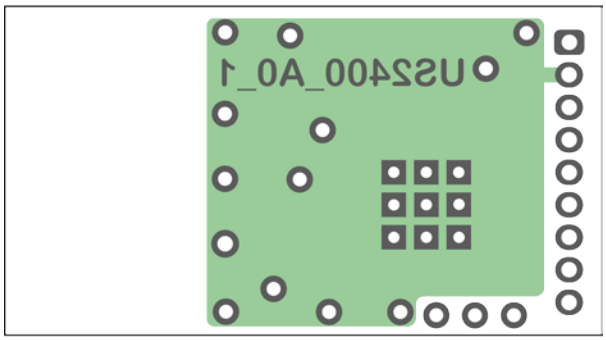
on a scale of 3:1

PCB top view



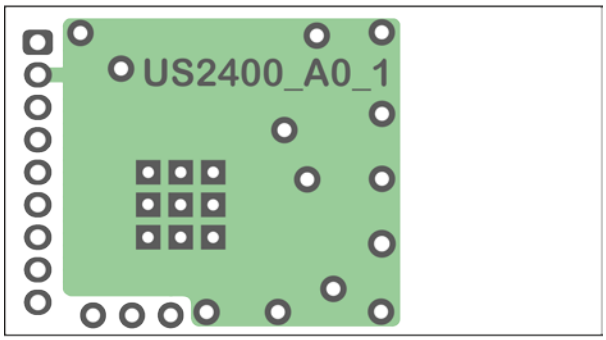
Board size: 23.7mm(X) / 13.2mm(Y)

PCB bottom view



Board size: 23.7mm(X) / 13.2mm(Y)

PCB bottom side



Board size: 23.7mm(X) / 13.2mm(Y)

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