UZ2400

Silicon Version D

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

Datasheet

DS-2400-51

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UZ2400

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

Applications

- ❑ Home/Building/Factory Automation
- ❑ 2-way Medium-Data-Rate Application
- ❑ Wireless Sensor Network
- ❑ PC Peripheral
- ❑ RF Remote Controller
- ❑ Consumer Electronics
- ❑ Low Power Wireless Communication
- ❑ Advanced Meter Infrastructure (AMI)

Introduction

UZ2400 Silicon Version D is a solution that complies with IEEE 802.15.4-2006 specifications. It integrates a 2.4 GHz RF transceiver with an IEEE802.15.4 compliant Baseband/MAC block within a single chip. The UZ2400 can be controlled by a microprocessor (e.g. 8051) for low-data-rate applications such as home automation, industrial automation, consumer electronics, PC peripheral …etc. For medium-data-rate applications like wireless voice and image transmission, the UZ2400 provides 1M/2M bps turbo mode.

The RF block of the UZ2400 integrates receiver, transmitter, voltage-controlled oscillator (VCO), and phase-locked loop (PLL). It uses advanced radio architecture to minimize the external component count and the power consumption. The Baseband/MAC block provides the hardware architecture for both IEEE 802.15.4 compliant MAC and PHY layers. It mainly consists of TX/RX control, CSMA-CA controller, 'Superframe' constructor, security engine and digital signal processing module. The UZ2400 is fabricated with the 0.18μm advanced RFCMOS process and is sealed in a 40-pin QFN 6x6 mm^2 package.

Features

RF/Analog

- ❑ ISM band 2.405~2.480 GHz operation
- ❑ IEEE 802.15.4-2006 specification compliance
- ❑ -95 dBm sensitivity and 3 dBm max. input level
- ❑ 0 dBm typical output power and 40 dB TX power control range
- ❑ Differential RF input/output and integrated TX/RX switch
- ❑ Integrated low phase noise VCO, frequency synthesizer and PLL loop filter
- ❑ Integrated 32 MHz and 32.768 KHz oscillator drive.
- ❑ Integrated internal oscillator circuit
- ❑ 32 MHz reference clock output
- ❑ Digital VCO and filter calibration
- ❑ Integrated RSSI ADC and I/Q DACs
- ❑ Integrated DC-DC converter
- ❑ High receiver and RSSI dynamic range
- ❑ 1M/2M bps turbo mode supported

- ❑ Low current consumption, 16 mA in RX and 17.5 mA in TX mode
- ❑ 2.4 uA deep sleep mode
- ❑ Small 40-pin leadless QFN 6x6 mm^2 package
- ❑ 0.18 µm RF CMOS technology
- ❑ Low external component count

MAC/Baseband

- ❑ IEEE 802.15.4-2006 specification compliance
- ❑ Hardware CSMA-CA mechanism, automatic ACK response and FCS check
- ❑ Programmable 'Superframe' construction
- ❑ Functionally independent TX FIFOs, including beacon FIFO, transmit FIFO and GTS FIFOs
- ❑ Dual RX FIFOs
- ❑ Hardware security engine (AES-128)
- ❑ Various power saving modes
- ❑ Support all CCA modes and RSSI/LQI
- ❑ Simple four-wire SPI interface
- ❑ I^{2}C slave supported

Block Diagram

Figure 1 shows the block diagram of the UZ2400. It is composed of six blocks:

- ❑ PHY block
- ❑ Lower MAC block
- ❑ Memory block
- ❑ Security engine block
- ❑ Power management block
- ❑ Interfacing block

Detailed descriptions for each block will be described in Chapter 3 of this datasheet.

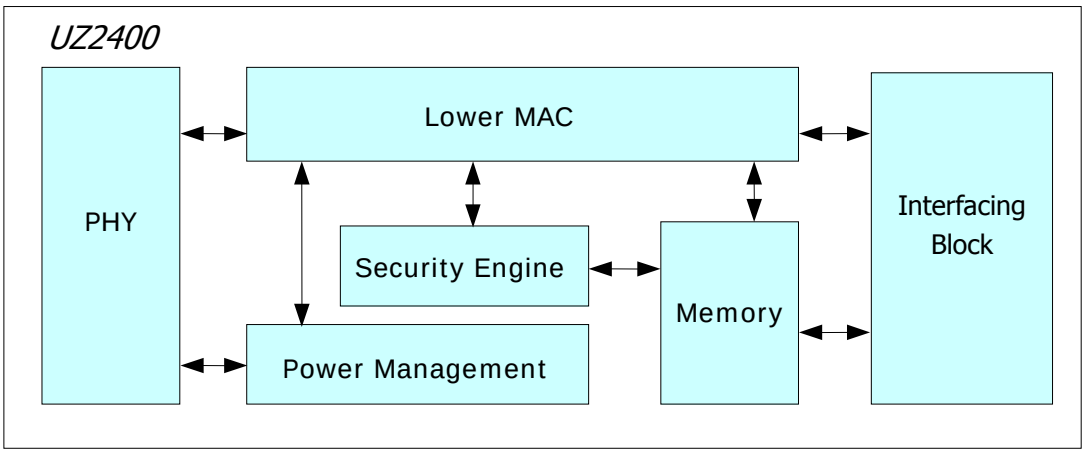

Figure 1: UZ2400 block diagram

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Abbreviations

ACK	Acknowledgement
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
CAP	Contention Access Period
CBC-MAC	Cipher Block Chaining Message Authentication Code
CCA	Clear Channel Assessment
CCM	Counter Channel Mode
CFP	Contention Free Period
CSMA-CA	Carrier Sense Multiple Access with Collision Avoidance
CRC	Cyclic Redundancy Check
CTR	Counter mode + CBC
DSSS	Direct Sequence Spread Spectrum
ESD	Electronic Static Discharge
EVM	Error Vector Magnitude
FCF	Frame Control Field
FCS	Frame Check Sequence
FIFO	First In First Out
GTS	Guaranteed Time Slot
IEEE	Institute of Electrical and Electronics Engineers
INT	Interrupt
ISM	Industrial Scientific and Medical
ITU-T	International Telecommunication Union - Telecommunication
I/O	Input / Output
I/Q	In-phase / Quadrature-phase
Kbps	Kilo bit per second
LNA	Low Noise Amplifier
LO	Local Oscillator
LQI	Link Quality Indication
LSB	Least Significant Bit / Byte
MSB	Most Significant Bit / Byte
MAC	Medium Access Control
MIC	Message Integrity Code
NA	Not Available
NC	Not Connected
O-QPSK	Offset Quadrature Phase Shift Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase Locked Loop
QFN	Quad Flat No-lead Package
RF	Radio Frequency
RSSI	Receive Signal Strength Indicator
RX	Receive

SPI	Serial Peripheral Interface
SFD	Start-of-Frame Delimiter
TBD	To Be Defined
TX	Transmit
VCO	Voltage Control Oscillator

Format Representations of Registers and their Bits

1. SREG0xnn[m] or SREG0xnn[p:m]
   SREG: short register
   0xnn: register number
   nn: can be numerical numbers (for example:1, 2, or 3, etc) or alphabetical words (for example: A, b, or C, etc)
   [m]: the bit number
   [p:m]: bit m, bit n, bit o, and bit p (for example: bit[7:5] means bit 7, bit 6, bit 5, and bit 4)

2. LREG0xnn[m] or LREG0xnn[p:m]
   LREG: long register
   0xnn: register number
   nn: can be numerical numbers (for example:1, 2, or 3, etc) or alphabetical words(for example: A, b, or C, etc)
   [m]: the bit number
   [p:m]: bit m, bit n, bit o, and bit p (for example: bit[7:5] means bit 7, bit 6, bit 5, and bit 4)

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1. Pin Configuration

1.1. Device Pin Assignments

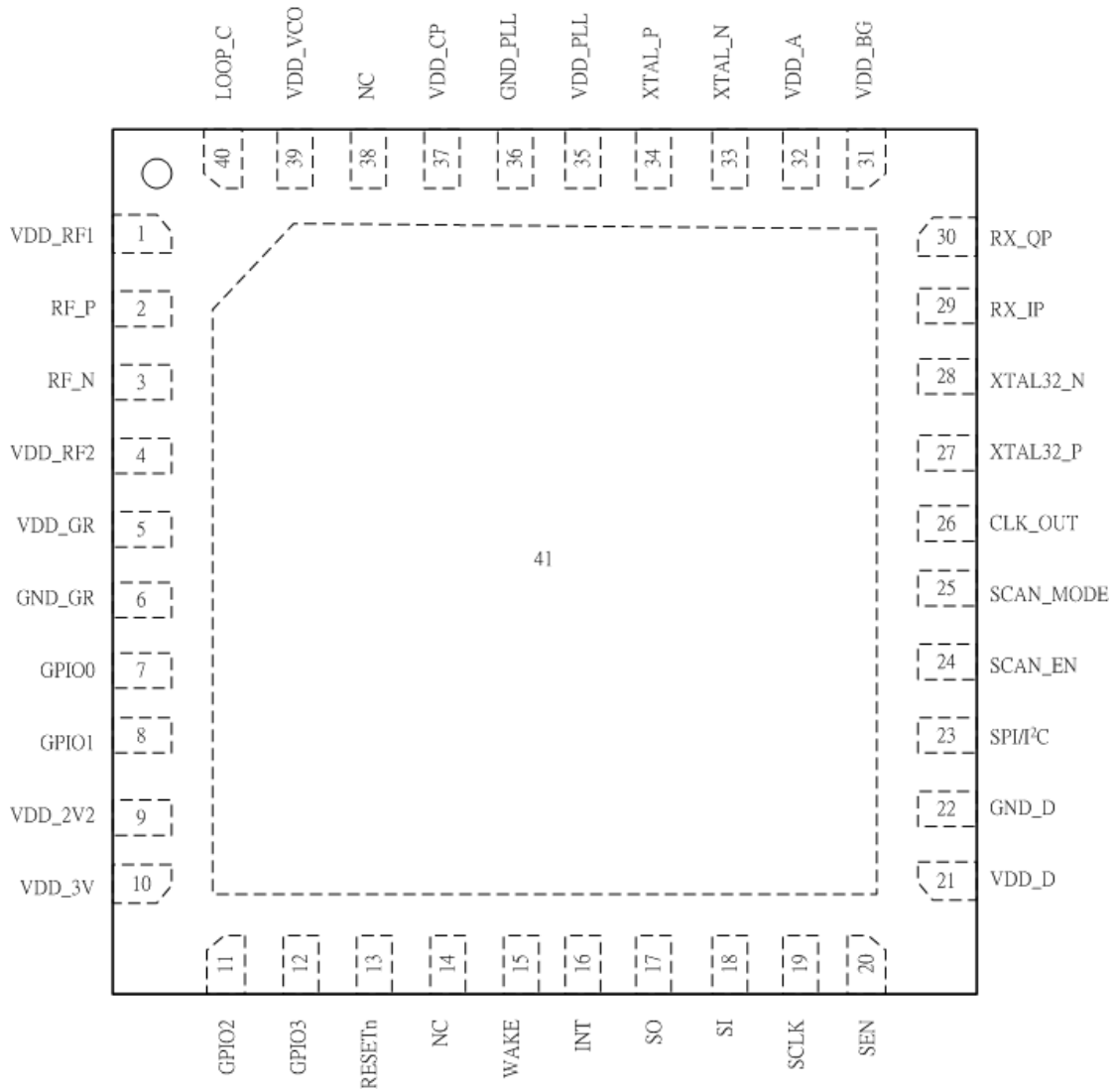


Figure 2: Pin assignments (top view)

1.2. Device Pin Descriptions

Pin type abbreviation: A = Analog, D = Digital, P = Power, I = Input, O = Output

Pin	Symbol	Type	Description
1	VDD_RF1	PI	RF power supply (1)
2	RF_P*	AIO	Differential RF input/output (+)
3	RF_N*	AIO	Differential RF input/output (-)
4	VDD_RF2	PI	RF power supply (1)
5	VDD_GR	PI	Guard ring power supply (1)
6	GND_GR	Ground	Guard ring ground
7	GPIO0	DIO	General purpose digital I/O; also used as an external PA enable
8	GPIO1	DIO	General purpose digital I/O; also used as an external TX/RX switch control
9	VDD_2V2	PO	DC-DC Converter output
10	VDD_3V	PI	DC-DC Converter input and I/O PAD power supply (1)
11	GPIO2	DIO	General purpose digital I/O, also used as an external TX/RX switch control
12	GPIO3	DIO	General purpose digital I/O
13	RESETn	DI	Global hardware reset pin, active low
14	NC		Not connected
15	WAKE	DI	External wake up trigger
16	INT	DO	Interrupt pin to microprocessor
17	SO/SCL	DIO	Serial interface data output from the UZ2400 or I2C clock
18	SI/SDA	DIO	Serial interface data input to the UZ2400 or I2C data in/out
19	SCLK	DI	Serial interface clock
20	SEN	DI	Serial interface enable
21	VDD_D	PI	Digital circuit power supply
22	GND_D	Ground	Ground for digital circuit
23	SPI/I2C	DI	SPI or I2C interface selection
24	SCAN_EN	DI	Scan insertion testing enable signal
25	SCAN_MODE	DI	Digital scan/test mode enable signal for chip testing purpose
26	CLK_OUT	DO	32 / 16 / 8 / 4 / 2 / 1 MHz Clock output (2)
27	XTAL32_P	AI	32.768 kHz Crystal input (+)
28	XTAL32_N	AI	32.768 kHz Crystal input (-)
29	RX_IP	AO	Analog RX I channel output (+)
30	RX_QP	AO	Analog RX Q channel output (+)
31	VDD_BG	PI	Power supply for bandgap reference circuit (1)
32	VDD_A	PI	Power supply for an analog circuit (1)
33	XTAL_N	AI	32 MHz Crystal input (-)
34	XTAL_P	AI	32 MHz Crystal input (+)
35	VDD_PLL	PI	PLL power supply (1)
36	GND_PLL	Ground	Ground for a PLL
37	VDD_CP	PI	Charge pump power supply (1)
38	NC		Not connected
39	VDD_VCO	PI	VCO power supply (1)

40	LOOP_C	AIO	PLL loop filter external capacitor. Connected to the external 39 pF capacitor.
41	IC ground pad	Ground	Backside ground plane. Must be connected to the ground.

Table 1: Pin descriptions

* ***Caution***: ESD sensitive. Please refer to Section 2.5 for more information.

Note 1: Connecting bypass capacitor(s) as close to the pin as possible.
Note 2: There is a risk of producing glitch on CLK_OUT pin when setting SREG0x2A[0] or LREG0x207[7:5].

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Parameters	Min	Max	Unit
Storage temperature	-40	+120	°C
Supply voltage VDD pin to the ground	-0.5	+3.8	V
Voltage applied to inputs	-0.5	+3.8	V
Short circuit duration, to GND, or VDD		5	sec

Table 2: Absolute maximum ratings

2.2. Recommended Operating Conditions

Test conditions: VDD = 3 V

Parameters	Min	Typ	Max	Units
Ambient Operating Temperature	-40		+85	°C
Supply Voltage for VDD_3V (*)	1.8	3	3.6	V
Logical high input voltage (for DI type pins)	0.8 x VDD_3V		VDD_3V	V
Logical low input voltage (for DI type pins)	0		0.2 x VDD_3V	V

Table 3: Recommended operating conditions

* Note 1: DC-DC Converter should be bypassed if supply voltage is below 2.0V. Please refer to Section 3.4.2.

* Note 2: The performances of output power and sensitivity at VDD=1.8V with DC-DC bypass are slightly different from the typical values. Please refer to Figure A-4 and Figure A-8 of Appendix A for details.

2.3. DC Electrical Characteristics

Test conditions: T_A = 25°C, VDD = 3 V

Chip Mode	Condition		Min	Typ	Max	Unit
ACTIVE: TX	At 0 dBm output power	DC-DC ON*		19.3		mA
		DC-DC OFF*		25.5		mA
ACTIVE: RX	Normal Mode (250 Kbps)	DC-DC ON*		17.5		mA
		DC-DC OFF*		20.4		mA
	Turbo Mode (1M/2M bps)	DC-DC ON*		20.0		mA
		DC-DC OFF*		23.3		mA
IDLE	MAC/BB, system clock and the sleep clock remain active RF circuit shutdown			6		mA
HALT	System clock, 1 MHz clock output and the sleep clock remain active RF/MAC/BB shutdown			1.8		mA
	System clock, 2 MHz clock output and the sleep clock remain active RF/MAC/BB shutdown			1.9		mA

	System clock, 4 MHz clock output and the sleep clock remain active RF/MAC/BB shutdown		2.0		mA
	System clock, 8 MHz clock output and the sleep clock remain active RF/MAC/BB shutdown		2.1		mA
	System clock, 16 MHz clock output and the sleep clock remain active RF/MAC/BB shutdown		2.4		mA
	System clock, 32 MHz clock output and the sleep clock remain active RF/MAC/BB shutdown		3.1		mA
STANDBY	Sleep clock remains active. RF/MAC/BB, system clock shutdown.		5.1		uA
DEEP SLEEP	Power to digital circuit remains active to retain Registers and FIFOs All the other power is shutdown.		4		uA
POWER DOWN	Minimum wake-up circuit remains active. All power is shutdown. Register and FIFO data are not retained.		0.1		uA

* Refer to Section 3.4.2

2.4. Radio Frequency AC Characteristics

2.4.1. Receiver Radio Frequency AC Characteristics

Test conditions: TA = 25°C, VDD = 3 V, LO frequency=2.445 GHz, DC-DC ON

Parameters	Condition		Min	Typ	Max	Unit
RF input frequency	Compatible to IEEE802.15.4-2006, 250 Kbps		2.405		2.480	GHz
RF sensitivity	At antenna input with O-QPSK signal	250 Kbps		-95		dBm
		1 Mbps		-85		dBm
		2 Mbps		-82.5		dBm
Maximum RF input			3			dBm
Adjacent channel rejection	@+/-5 MHz, 250 Kbps			24		dB
Alternate channel rejection	@+/-10 MHz, 250 Kbps			40		dB
RSSI range	Normal mode (250 Kbps)			44		dB
	Turbo mode (1M/2M bps)			43		dB

2.4.2. Transmitter Radio Frequency Characteristics

Test conditions: T_A = 25°C, VDD = 3 V, LO frequency=2.445 GHz, 250 Kbps, DC-DC ON

Parameters	Condition	Min	Typ	Max	Unit
RF carrier frequency	Compatible to IEEE802.15.4-2006	2.405		2.480	GHz
Maximum RF output power	At 0 dBm output power setting	-3	0		dBm
RF output power control range			40		dB
TX gain control resolution		0.1		0.5	dB
TX spectrum mask for O-QPSK signal	Offset frequency > 3.5 MHz			-30	dBm
	At 0 dBm output power	20			dBc
TX EVM			12		%

2.5. ESD Notice

Human-body mode → All pins pass 2KV
Machine mode → Pin2, 3 ESD sensitive, pass 100V, other pins pass 200V
CDM mode → Pin33, 34 pass 400V, other pins pass 700V

2.6. Peripheral Characteristics

The UZ2400 has both a SPI slave mode and I^2C interfaces. They can be used by the MCU host to access the registers of the UZ2400 and FIFOs. The 4-wire SPI (SEN, SCLK, SI, and SO) provides a high speed interface up to 5 MHz on SCLK. Also, the 2-wire I^2C (SDA and SCL) interface provides another lower pin-count solution. The I^2C SDA and SCL share the same pins with SPI SI and SO respectively.

The UZ2400 has four GPIO pins. Each can be configured either as an input or an output pin.

2.7. Power-on and Reset Characteristics

The UZ2400 has built-in power-on reset (POR) circuit which automatically resets all digital registers when the power is turned on. The 32 MHz oscillator circuit starts to lock frequency of the right clock after power-on. The whole process takes 3ms for a clock circuit to become stable and completes the power-on reset. It is highly recommended that the user waits at least 3ms before starting to access the UZ2400.

For external hardware reset (warm start), external reset pin RESETn is internally pulled-high. The UZ2400 will hold in reset state around 20usec after RESETn is released from the low state.

2.8. Crystal Parameter Specifications

The clock system of the UZ2400 can be separated into two parts, one is main clock and the other is sleep clock. The main clock is generated by a 32 MHz oscillator while the sleep clock can be selected between 32.768 KHz oscillator and internal oscillator. Among all, the 32 MHz and 32.768 KHz clocks utilize external crystals to generate the oscillations. The associated pins are XTAL_P, XTAL_N for 32 MHz crystal; the pins XTAL32_P and XTAL32_N are for 32.768 KHz crystal. The allowed variation in frequency for the 32 MHz crystal is from -40ppm to +40ppm. The 32.768 KHz clock provides real-time-clock based time accuracy to count sleep duration.

3. Functional Description

The UZ2400 is composed of the following six blocks:

- PHY block
- Lower MAC block
- Memory block
- Power management block
- Security block
- Interfacing block

The block diagram of the UZ2400 is shown in Figure 3. Each of the blocks will be described later in this Chapter.

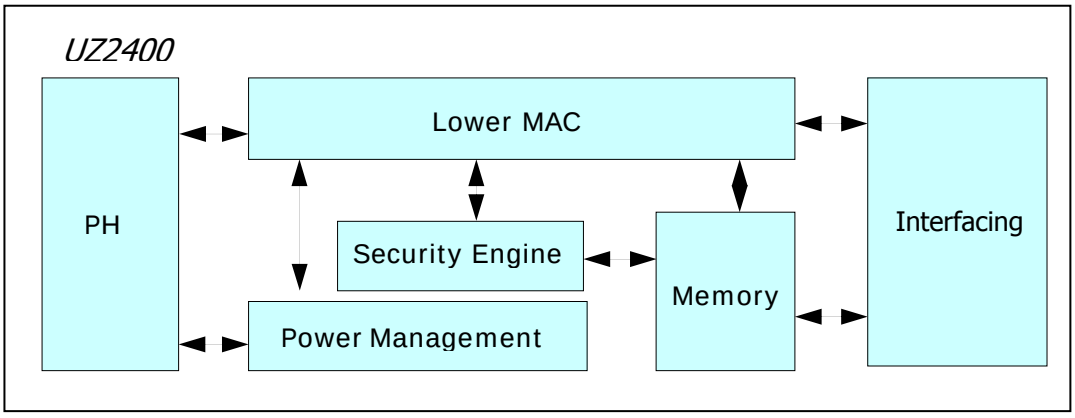


Figure 3: the block diagram of the UZ2400

3.1. PHY Block

The PHY (physical) block is compliant to IEEE 802.15.4-2006 2.4GHz ISM band standard. The architecture is shown in Figure 4.

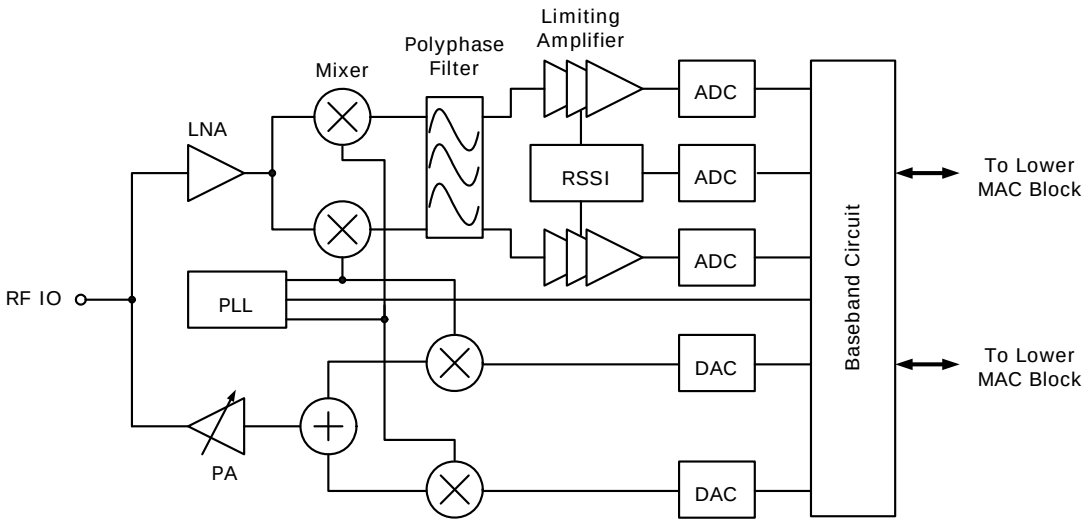


Figure 4: PHY block architecture

3.1.1. IEEE 802.15.4-2006 PHY Introduction

Although a brief introduction of IEEE 802.15.4-2006 PHY layer is available in this section, it is recommended that user should read the specification of IEEE 802.15.4-2006 for more comprehensive understanding.

The UZ2400 provides a transceiver which is fully compatible to IEEE 802.15.4-2006 2.4GHz band PHY layer specifications. The key features of the IEEE 802.15.4-2006 PHY layer are described as below.

- Operating frequency range is from 2405 to 2480 MHz, which includes 16 channels.
- It uses Offset QPSK (OQPSK) modulation to transmit data at 250kbps.
- Direct Sequence Spreading Spectrum (DSSS) is used in baseband algorithm to increase the SNR.
- It provides clear channel assessment (CCA) for CSMA-CA function.
- RSSI signal strength indicator is also provides.

The IEEE 802.15.4-2006 compliant packet includes a 6 bytes PHY header and a 5~127 bytes PHY payload. The 6 bytes PHY header includes 4 bytes of preamble, 1 byte of start-of-frame delimiter (SFD), and 1 byte of payload length. Preamble and SFD are used for receiver packet detection and synchronization. The payload length is valid from 5 to 127 for an IEEE 802.15.4-2006 compliant packet.

The PHY payload includes variable bytes of MAC header, variable bytes of MAC payload and 2 bytes of cyclic redundant check (CRC, also called frame check sequence, FCS). The packet format is as below:

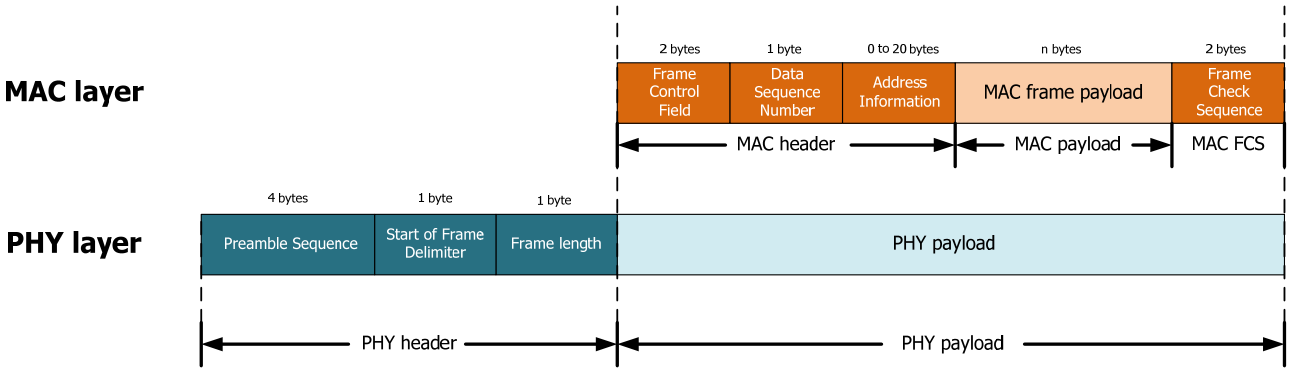


Figure 5: PHY layer frame format

For more information, please refer to IEEE 802.15.4-2006 standard.

3.1.2. The PHY Enhancement of the UZ2400

Other than IEEE 802.15.4-defined 250Kbps data rate, 1M/2M bps turbo modes are supported in UZ2400. Under turbo mode, users can use the same program settings for MAC. All MAC functions including auto-ACK, CSMA-CA, Superframe… etc. are remained the same. To change to turbo modes, please refer to Section 4.3.6.

In both 1M/2M bps modes, signal bandwidth is extended to 8MHz.

UZ2400 uses a fractional-N PLL as frequency synthesizer. Therefore, the carrier frequency resolution increases and 1MHz channel spacing can be supported. Users can program UZ2400 to any integer carrier frequency between 2400MHz and 2495MHz.

3.1.3. RSSI/ED and LQI

RSSI is used to report the signal strength of a received packet. The UZ2400 is able to automatically attach LQI and RSSI values following a received packet in RXFIFO every time a packet is received successfully. The data format in RXFIFO is as below:

RXFIFO Address					
0x300				0x300+m+n+3	0x300+m+n+4
1 Byte	M Byte	N Bytes	2 Byte	1 Byte	1 Byte
Frame length	MAC Header	MAC Payload	MAC FCS	LQI	RSSI

For more information about RXFIFO, please refer to Section 3.3.2.

3.1.4. CCA

Clear Channel Assessment (CCA) is designed to detect whether the current channel is occupied by other devices and used in the CSMA-CA algorithm (see Section 3.2.5). The UZ2400 provides three types of CCA functions: CS (Carrier Sense), ED (Energy Detection) and a combination of both.

- CS mode: The CCA/CS mode, which is the default of CCA, detects if there is an IEEE 802.15.4 2.4GHz OQPSK signal occupying the current channel. To use this mode, set SREG0x3A[7:6] to '0b01' and then configure the CS threshold by setting the short register SREG0x3A[5:2].
- ED mode: The CCA/ED mode detects if there is an in-band signal occupying the current channel. To use this mode, set SREG0x3A[7:6] to '0b10' and then configure the ED threshold by setting the short register SREG0x3F. The current consumption of RSSI circuit is around 2.3 mA. It is recommended to set CCA to ED mode before setting the trigger bit of TXFIFO to send the packet and to set CCA back to CS mode after the interrupt status is read. The detailed procedure is given in Section 4.4.4.
- Combination of CS and ED mode: This mode checks both the CS and ED results for CCA. CCA shall report a busy medium only upon the detection of a signal with the modulation and spreading characteristics of IEEE 802.15.4 with energy above the Energy Detection (ED) threshold. To use this mode, set the short register SREG0x3A[7:6] to '0b11' and set the CS and ED threshold as described above.

3.2. Lower MAC Block

The UZ2400 MAC provides plenty of hardware-assisted features to relieve the host MCU power requirement.

TXMAC performs the CSMA-CA protocol to send a packet automatically. It also generates a 16-bit FCS automatically. In Beacon-enabled mode, according to the 'Superframe' architecture, a TXMAC will send the packet in Normal FIFO during the CAP (contention access period), the packet in GTS1/GTS2 FIFO during the CFP (contention free period) and the packet in beacon FIFO during the 'Superframe' beacon period.
RXMAC receives packets from the RX Baseband. The received packet is put into a RXFIFO and the FCS of the

packet is checked for validity simultaneously. RXMAC performs the packet filtering with both of the destination address field and PANID. If both of them match their own identity and the FCS check is passed, an interrupt is issued to the host MCU. Unqualified packets are skipped. RXMAC also informs a TXMAC to send an acknowledge packet automatically. This happens whenever a packet is successfully received and the bit 5 of FCF is set to '1'. This will maintain the time requirement of the acknowledged packet.

A 16-bit MAC timer is provided to facilitate the generation of the 15.36 ms interrupt for the ZigBee Network.

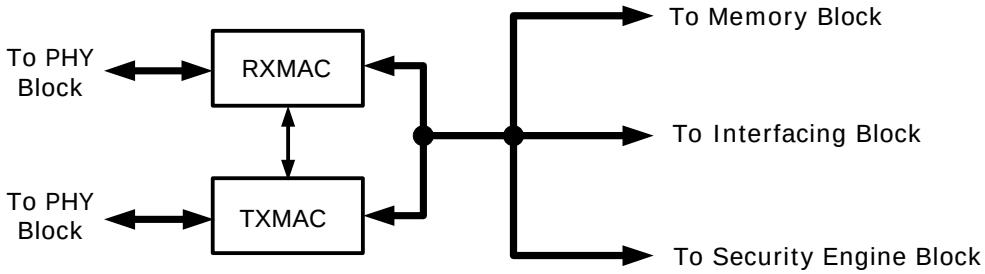


Figure 6: Lower MAC block diagram

3.2.1. IEEE 802.15.4-2006 MAC Introduction

Although a brief introduction of IEEE 802.15.4-2006 MAC layer is available in this section, it is recommended that user should read the specification of IEEE802.15.4-2006 for more comprehensive understanding.

The IEEE802.15.4 MAC layer provides reliable wireless packet transactions between two nodes. It also handles data and command transfer between the network and the physical layers. It handles the following tasks:

- Generating network beacons
- Synchronizing to beacons
- Supporting PAN association and disassociation
- Employing the CSMA-CA mechanism for channel access
- Handling and maintaining the guaranteed time slot mechanism
- Providing a reliable link between two peer MAC entities

The packet format of PHY and MAC layer is given below:

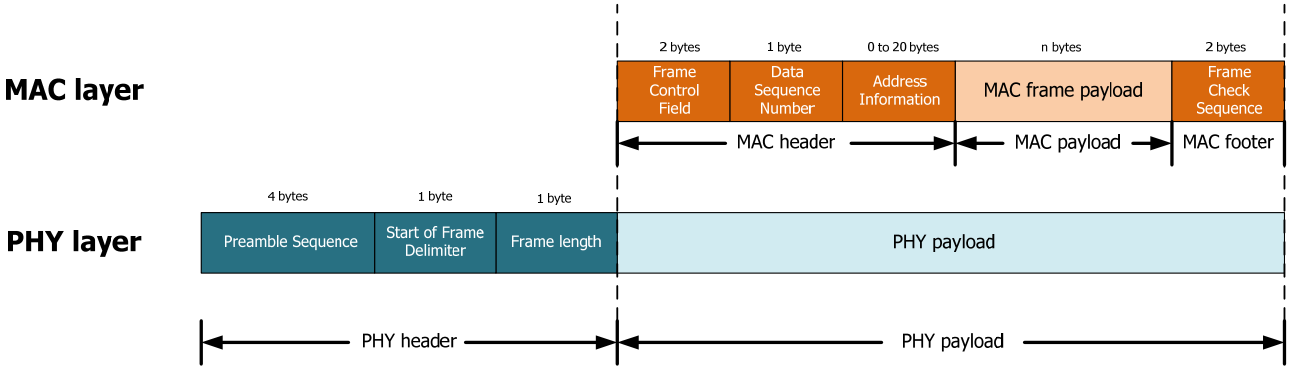


Figure 7: Packet format for PHY and MAC

The frame control field (FCF) format is two bytes:

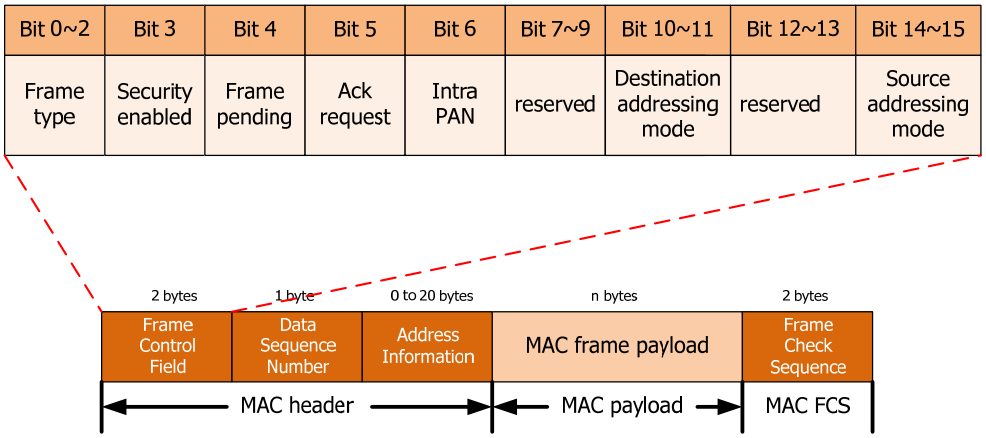


Figure 8: MAC frame control field

The frame check sequence (FCS) is CRC-16. The polynomial is degree 16:

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1$$

A PAN may be set up in one of the two basic configurations: Beacon-enabled and Non-Beacon-enabled. In a Non-Beacon-enabled network, devices may communicate with each other at any time after an initial association phase. Contention-based channel access is managed using a non-slotted CSMA-CA mechanism and any node-level synchronization must be performed at some higher layer. In a Beacon-enabled network, the PAN coordinator periodically transmits a beacon which other devices use for both the synchronization and the determination of the time when to enable transmission and reception of messages. This beacon message is used to define a 'Superframe' structure that all nodes in the PAN should synchronize to. This 'Superframe' structure is shown in the following figure.

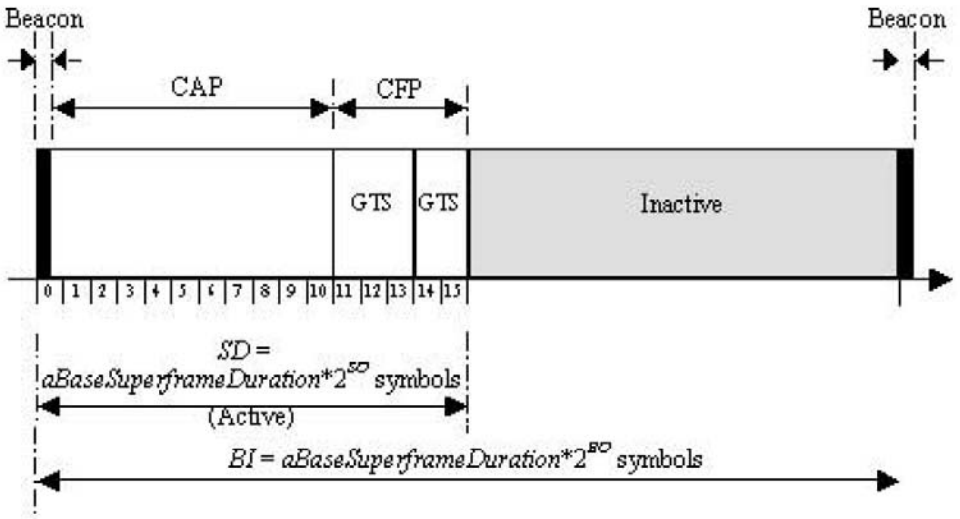


Figure 9: example of IEEE 802.15.4 MAC 'Superframe' structure

The 'Superframe' is divided into several sections whose lengths are configurable. There is an active period, during which the communication takes place, and an inactive period, during which the devices may turn off their transceivers in order to conserve the power. The active period is divided into 16 equally-spaced slots.

Immediately following the beacon is the contention access period (CAP). During this period, the devices may communicate using a slotted CSMA-CA mechanism. This is similar to the non-slotted CSMA-CA, except that the back-off periods are aligned with the slot boundaries, meaning that the devices are contending for the right to transmit over the entire slots. The CAP must contain at least nine time slots for an active period but may take up all 16.

Following the CAP is an optional contention free period (CFP), which may last up to seven time slots in an active period. In the CFP, the devices are allocated GTS slots by the PAN coordinator. During a GTS, a device has the exclusive access to the channel and does not perform CSMA-CA. During one of these GTSs, a device may either transmit data to or receive data from its PAN coordinator, but not both. The length of a GTS must be an integral multiple of an active period slot. All GTSs must be contiguous in the CFP and are located at the active period in the end of the 'Superframe'. A device may disable its transceiver during a GTS designated for another device in order to conserve power.

All devices must go through an initial association phase in order to become part of a PAN. This association is prompted by a higher layer service, but it uses primitives defined in the MAC to perform the associations. The MAC allows configurations to be set for starting a device as a PAN coordinator, allowing a coordinator to have devices associated with it and performing the actual association of a device with some coordinator.

Once becoming part of a PAN, the data sent between a device and its coordinator is performed in one of the ways shown in the following figure. Note that acknowledgments are optional in all the transfers from a device to its coordinator, but they are required in transfers from the coordinator to a device. When transferring from a coordinator to a device, the device must first request the data from the coordinator. In a Non-Beacon-enabled network, devices must poll the coordinator for data at an application-specified rate, as there are no beacons to notify the device that there is data pending for it.

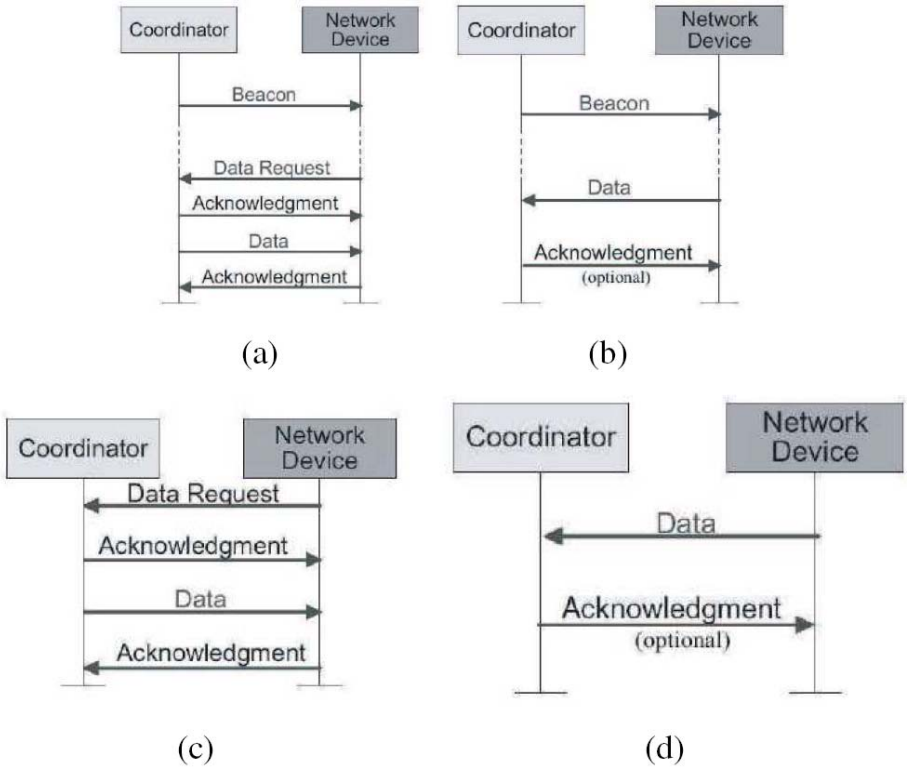


Figure 10: Data transfer between a coordinator and its devices
a) Coordinator to Device with Beacons enabled, b) Device to Coordinator with Beacons enabled
c) Coordinator to Device with Beacons disabled, d) Device to Coordinator with Beacons disabled

3.2.2. MAC Timer

The UZ2400 has an internal MAC timer for the use of the ZigBee protocol. It is a 16-bit down-counting timer ticking with MAC time of 8us period. The beacon interval for the ZigBee protocol can be set to multiple times of 15.36ms, which is 1920 times of 8us. Using a MAC timer can relieve the work load of the timer of the MCU. The MAC timer can be triggered by writing SREG0x29 to start downward counting. The timer generates a MAC timer interrupt when the down-counting reaches zero.

3.2.3. RXMAC

The RXMAC will do the CRC checking, parsing the received frame type and address recognition before storing the received frame in the RXFIFO which contains two 144-byte dual ports FIFOs, RXFIFO0, and RXFIFO1. The received frame will be stored in the RXFIFO one packet at a time. A byte of length will be extracted from the PHY header and be appended in the front of the MAC frame. This facilitates the MCU host to decode the frame correctly with correct frame length information. Moreover, there are other 2 bytes of information attached to the MAC frame - LQI and RSSI. Detailed descriptions of the RXFIFO are in Section 3.3.2.

The behaviors of a RXFIFO follow a certain rule: When a received packet is not filtered or dropped out, a RX interrupt/status will be issued to MCU host. The interrupt is a read-to-clear type to save the operation time of the MCU host. However, the contents of the RXFIFO can be flushed only by the following three ways: (1) the

MCU host reads length field of RXFIFO and the last byte of the packet, (2) the host issues a RX flush, and (3) the software reset. Note that RXFIFO is ready to receive next packet and all the data in RFIFO will be overwritten after RXFIFO flushed.

A RXMAC recognized a valid packet according to rules provided in Section 7.5.6.2 of the IEEE802.15.4-2006 specification. The acceptance rules are:

(1) The frame type subfields shall not contain an illegal frame type.
(2) If the frame type indicates that the frame is a beacon frame, the source PAN identifier shall match macPANId unless macPANId is equal to 0xFFFF, in which case the beacon frame shall be accepted regardless of the source PAN identifier.
(3) If a destination PAN identifier is included in the frame, it shall match macPANId or shall be the broadcast PAN identifier (0xFFFF).
(4) If a short destination address is included in the frame, it shall match either macShortAddress or the broadcast address (0xFFFF). Otherwise, if an extended destination address is included in the frame, it shall match aExtendedAddress.
(5) If only source addressing fields are included in a data or MAC command frame, the frame shall be accepted only if the device is a PAN coordinator and the source PAN identifier matches macPANId.

If the above conditions are met, a RXMAC will issue a RX interrupt to indicate a valid packet is received.

The UZ2400 RXMAC supports an automatic ACK reply. If and only if the five conditions mentioned above are met, and an AckReq bit in the frame-control field of the header of the received packet is set, an ACK packet will be sent by a TXMAC automatically. The sequence number will be the same as incoming packet.

When an encrypted packet is received, RXMAC will not inform the security module directly. Instead, it issues a security interrupt to the MCU host. Then the MCU host can decide whether to decrypt or ignore it.

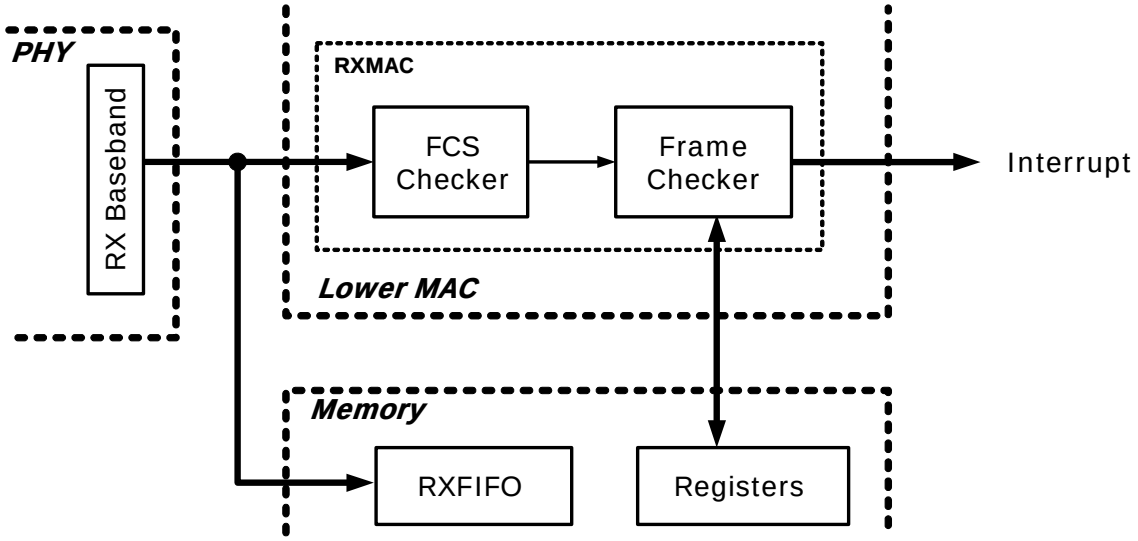
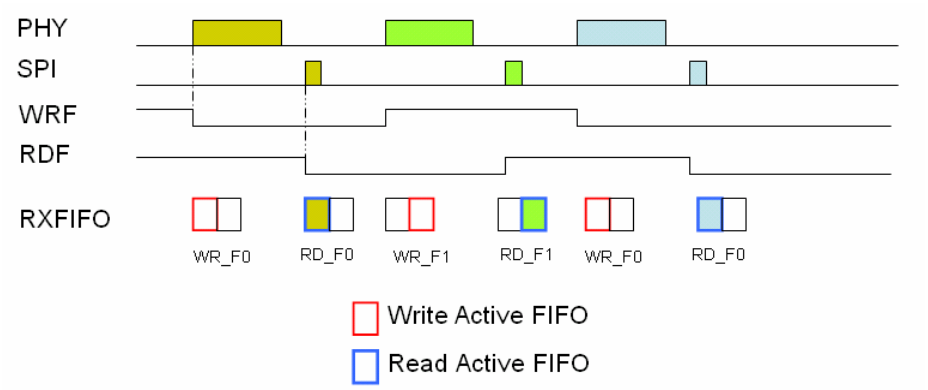
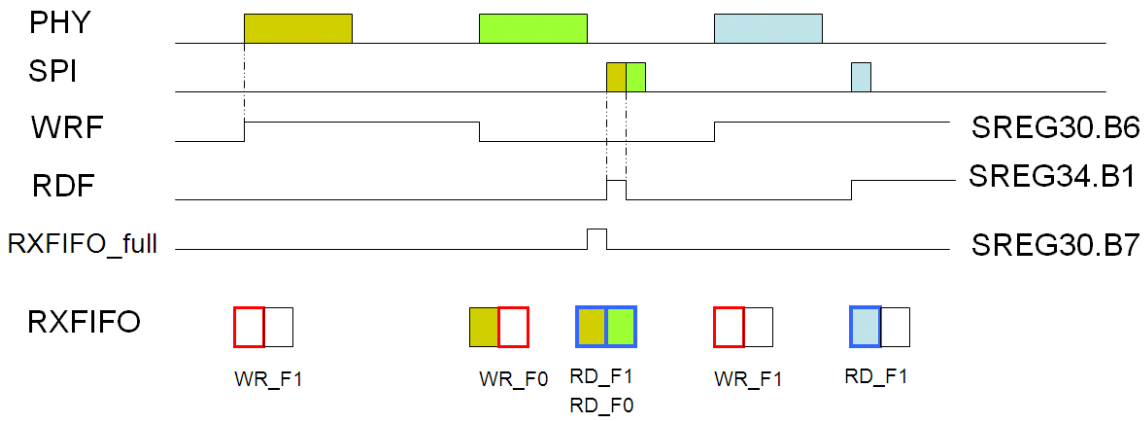


Figure 11: RXMAC block diagram

Two Ping-Pong FIFOs, RXFIFO0 and RXFIFO1 are mapped to the long address memory space from '0x300' to '0x38F'. The UZ2400 supports the Ping-Pong receiving process utilizing the two FIFOs. This receiving process is called Ping-Pong RX mode. Each FIFO has 144-byte memory with two ports. SREG0x34[0] can enable Ping-Pong FIFO mode, which is disabled by default. RXMAC automatically switches between RXFIFO0 and RXFIFO1 whenever a new packet comes.

An RX interrupt will be issued after the complete frame is stored in a RXFIFO. For Ping-Pong RX mode, when the MCU host read the first byte of the long address memory '0x300', the RXMAC will change the read flag SREG0x34[1] automatically. For manually controlled RX operation, if the value of the read flag SREG0x34[1] is 0, the register file RXFIFO0 will be read. Otherwise, if the value of the read flag SREG0x34[1] is 1, the register file RXFIFO1 will be read.





In the above diagram, the current status of each frame is represented as the register SREG0x30. SREG0x30[7] means 'RXFIFO full' indicating the two RXFIFOs are occupied. If the MCU host cannot read the RXFIFO in time, the value of SREG0x30[7] will be set to 1, and the value of SREG0x30[6:1] will be updated. Then the last status of the RX frame will be kept in SREG0x33. Once the MCU host read the RXFIFO, the value of the SREG0x30[7] will be set to 0 automatically.

3.2.4. TXMAC

The block diagram of a TXMAC is shown in the Figure 12 below. The TXMAC performs three major tasks that conform to the IEEE 802.15.4 standard. They are:

- TXFIFO control
- Automatic CSMA-CA and time alignments.
- Hardware 'Superframe' handling.

For a TXFIFO control function, TXMAC controls four FIFOs including the beacon, normal and two GTS FIFOs. When each of the FIFOs is triggered, the TXMAC performs the CSMA-CA algorithm, sends the packet to the PHY layer of the TX at the right time, handles the retransmission if an ACK is required but not received, and generates FCS bytes automatically. An automatic CSMA-CA algorithm performs the time alignments such as LIFS, SIFS and ACK turnaround time. A user can simply use the parameters of CSMA-CA algorithm and the TXMAC will perform corresponding tasks automatically.

For hardware, the 'Superframe' handling under the operation, the TXMAC builds up the time frame of a 'Superframe' automatically. This greatly alleviates the loading of the upper MCU. The TXMAC calculates the time for CAP, CFP, INACTIVE and each time slot then perform corresponding task if there is any. The TXMAC sends the beacon, normal and GTS FIFOs at the right time of each transmission automatically. This largely reduces the complexity of Beacon-enabled mode of IEEE 802.15.4.

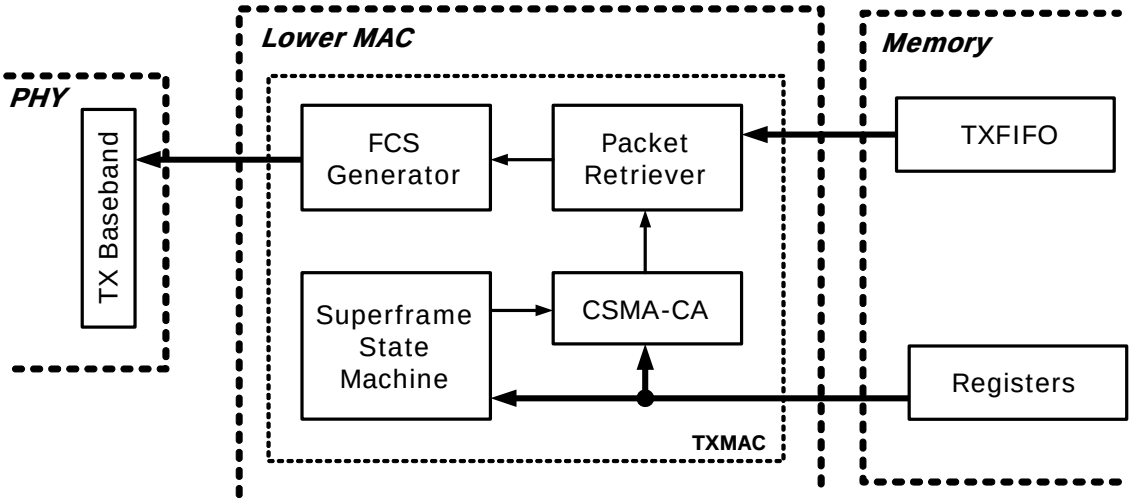


Figure 12: TXMAC block diagram

3.2.5. CSMA-CA

The Low-Rate Wireless Personal Area Network (LR-WPAN) uses two types of channel access mechanism, un-slotted CSMA-CA and slotted CSMA-CA. This depends on the network configuration. Non-Beacon-enabled network uses an un-slotted CSMA-CA while beacon-enabled network uses a slotted CSMA-CA.

For the non-slotted CSMA-CA, each time a device wishes to transmit data frames or MAC commands, it will wait for a random back-off. If the device finds that the channel is idle, it will wait for another extra random back-off

before transmitting its data. This extra random back-off reduces the chance of an on-air data collision. If a channel is busy, the device will try to access the channel again following a random back-off. Once the device finds that the channel becomes idle, it will wait for another extra random back-off before transmitting its data. If the channel is always busy and the times of failure is more than macMaxCSMABack-offs (defined in IEEE 802.15.4, this parameter equals 4 by default), the process is considered failed. Acknowledgment frames will be sent without using a CSMA-CA mechanism.

User can modify the parameters of the CAMA-CA of the UZ2400 as follow.

- SREG0x0d[3] defines whether the CSMA-CA algorithm of normal FIFO is used or not. SREG0x11[7] defines whether the CSMA-CA algorithm of GTS FIFO is used or not. Setting SREG0x0d[3] or SREG0x11[7] to '1' disables the CSMA-CA algorithm for normal FIFO or GTS FIFO, otherwise else.
- SREG0x11[4:3] defines the minimum value of the back-off exponent in the CSMA-CA algorithm. Note that if this value is set to 0, the collision avoidance is disabled during the first iteration of the algorithm. Also note that for the slotted version of the CSMA-CA algorithm with the battery life extension enabled, the minimum value of the back-off exponent will be the lesser of 2 and the value of macMinBE*.
- SREG0x11[2:0] defines the maximum number of back-offs which the CSMA-CA algorithm will attempt before declaring a channel access failure. The range is between 0 and 5.

*: macMinBE - a variable of the IEEE 802.15.4

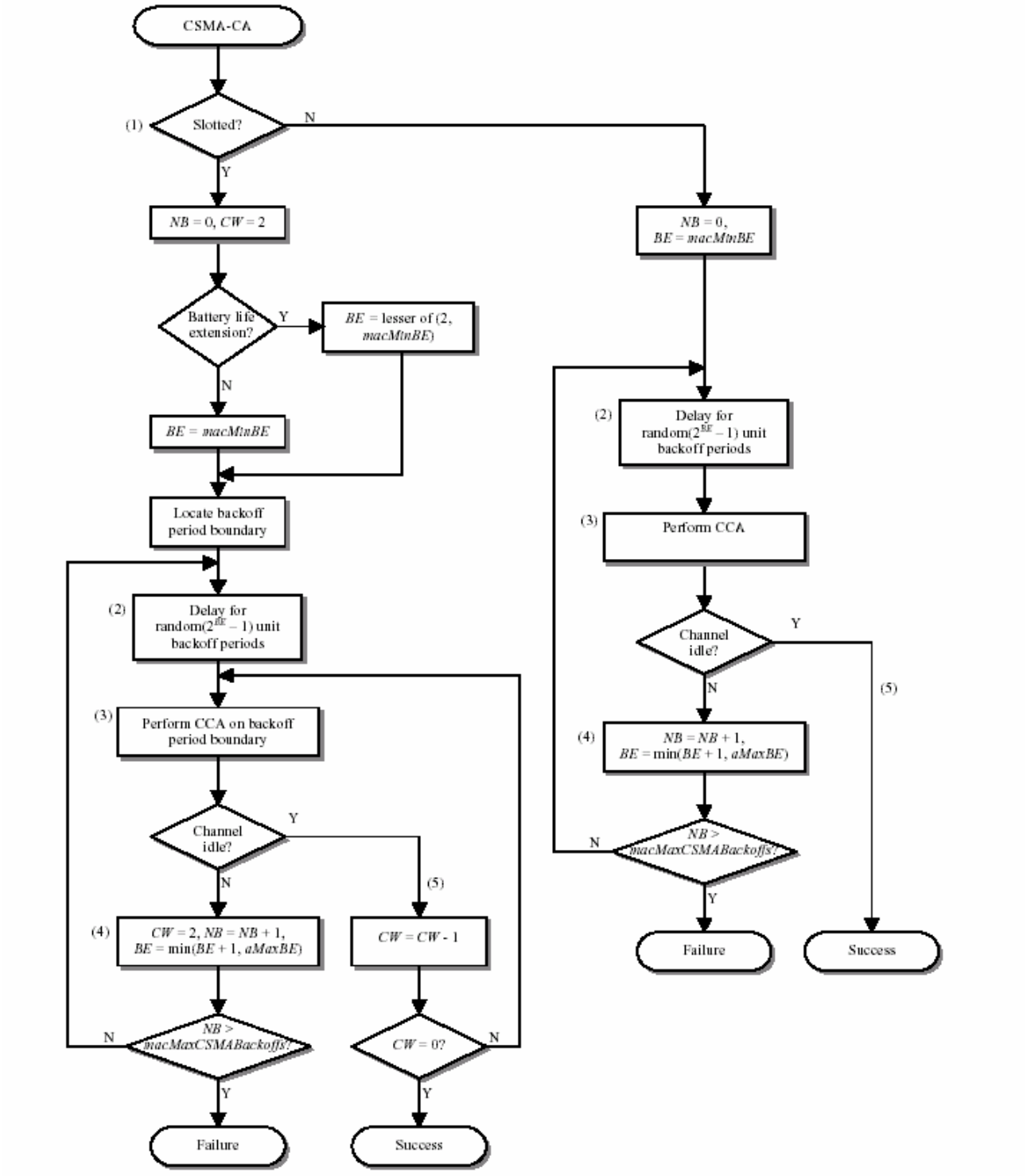


Figure 13: CSMA-CA algorithm

3.3. Memory Block

The memory block (including registers and FIFOs) of the UZ2400 is implemented by the SRAM. It is composed of registers and FIFOs shown as below:

Registers

- Short address register (6-bit short addressing mode register, total 64 bytes)
- Long address register (10-bit long addressing mode register, total 128 bytes)

FIFOs

- TX FIFO – Normal (128 bytes)
- TX FIFO – Beacon (128 bytes)
- TX FIFO – GTS1 (128 bytes)
- TX FIFO – GTS2 (128 bytes)
- Security Key FIFO (64 bytes)
- RX FIFO – RXFIFO0 (144 bytes)
- RX FIFO – RXFIFO1 (144 bytes)

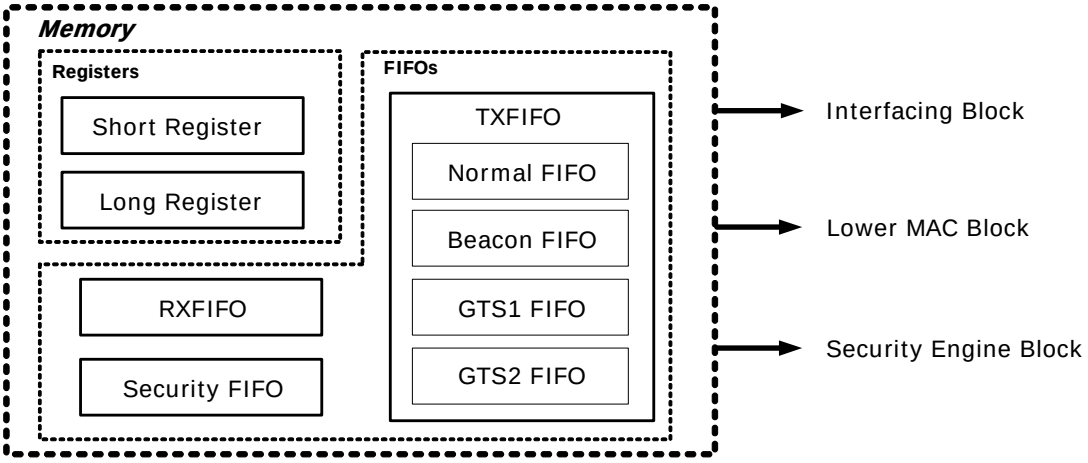


Figure 14: Memory block diagram

Registers provide control bits and status flags for the UZ2400 operations, including transmission, reception, interrupt control, timer, MAC/baseband/RF parameter settings, security … etc. Short address registers are accessed by short addressing mode with valid addresses ranging from '0x00' to '0x3F'. Long address registers are accessed by long addressing mode with valid addresses ranging from '0x200' to '0x27F'. Please refer to Section 3.7.1 and 3.7.2 for detailed addressing rules for SPI and I^2C interface.

FIFOs serve as the temporary data buffers for data transmission, reception and security keys. Each FIFO holds only one packet at a time. The transmission FIFO is called TXFIFO. A TXFIFO is composed of four 128-byte FIFOs for different purposes, namely Normal FIFO, Beacon FIFO, GTS1 and GTS2 FIFO. The receiving FIFO is called RXFIFO. A RXFIFO is composed of two 144-byte FIFO. The final part is called Security Key FIFO. The Security Key FIFO is composed of one 64-byte FIFO and is capable of holding four 16-byte security keys for secured operation. The beacon and GTS2 FIFOs share the same security key space. Please refer to Section 4.2 for further information about registers and FIFOs.

3.3.1. Registers

Short Address Registers

Short address registers are accessed by short addressing mode with valid addresses ranging from '0x00' to '0x3F'. Together with long registers, they provide control bits and status flags for the UZ2400 operations, including transmission, reception, interrupt control, timer, MAC/baseband/RF parameter settings, security, etc. Short registers are accessed faster than long registers.

Long Address Registers

Long address registers are accessed by long addressing mode with valid addresses ranging from '0x200' to '0x27F'. Together with short registers, they provide control bits and status flags for the UZ2400 operations, including transmission, reception, interrupt control, timer, MAC/baseband/RF parameter settings, security, etc. Long registers are accessed slower than short registers.

3.3.2. FIFOs

TXFIFO

The TXMAC gets data to transmit from four TXFIFOs: beacon, normal, GTS1 and GTS2. According to different conditions, different FIFO is selected. All four TXFIFOs are 128 bytes in length, which can contain one 802.15.4 MAC packet at a time.

In Non-Beacon-enabled mode, the TXMAC always gets data from Normal FIFO. In Beacon-enabled mode, the TXMAC gets data from the beacon FIFO during the beacon slot. It gets data from Normal FIFO during CAP slots and GTS1/GTS2 FIFOs during CFP slots. All of the four FIFOs can be accessed by SPI/I2C interface.

GTS1 and GTS2 FIFOs are Ping-Pong FIFOs. They are designed for QoS (quality of service) during Beacon-enabled mode. The two FIFOs can be assigned to different GTS slots. If they are in the same slot, they take turns within that GTS slot if both are triggered. The GTS1/GTS2 FIFO can be triggered before their GTS slot comes. Below is GTS FIFO's behavior:

Further information about the recommended typical operation steps of TXFIFO is available in Section 4.4.

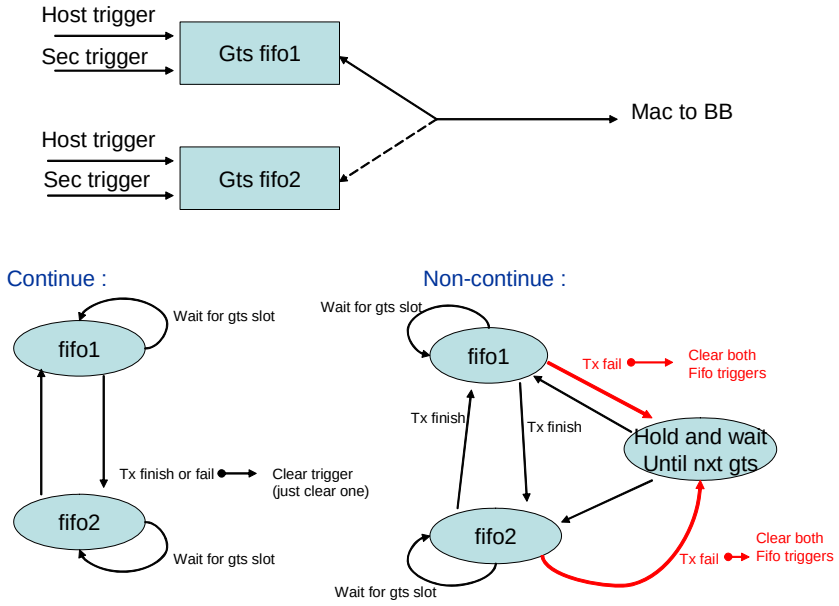


Figure 15: GTS FIFO selection

RXFIFO

A RXFIFO is composed of two 144-byte FIFOs (RXFIFO0 and RXFIFO1) to store the incoming packet. Each of them is designed to store one packet at a time. Section 3.2.3 details the RXMAC behavior.

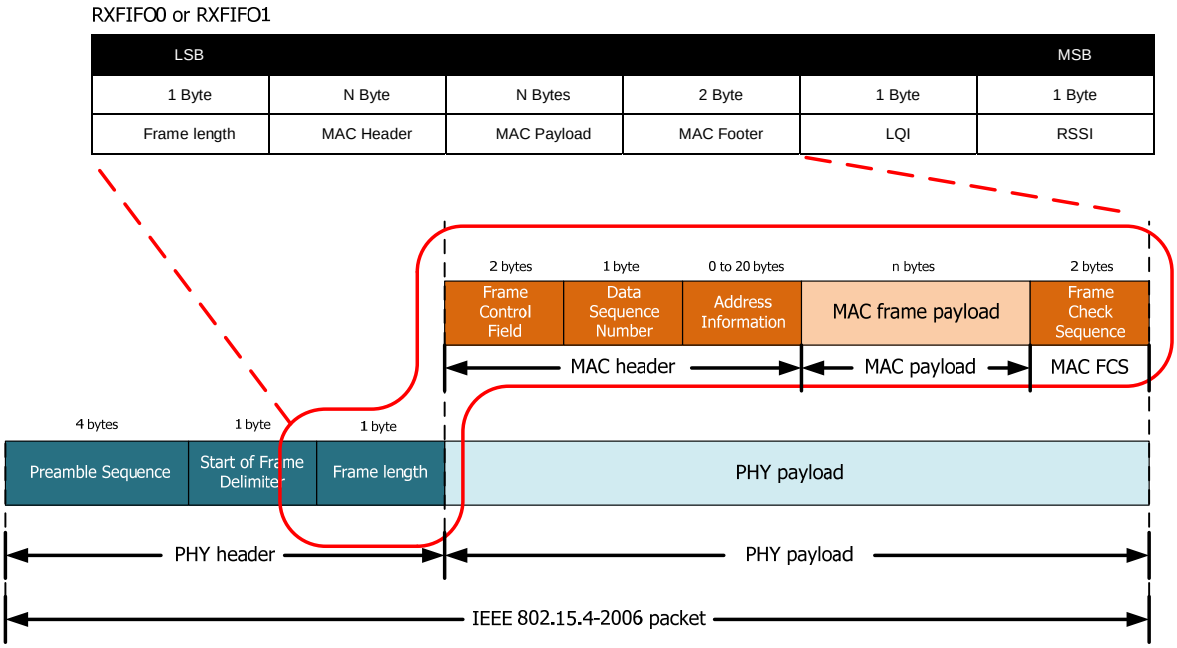


Figure 16: the relationships between RXFIFO and IEEE 802.15.4 packet

A frame records the length of the data in byte, including MAC header, MAC payload, and MAC FCS (MAC frame check sequence). The frame length does not include LQI (1 byte) and RSSI (1 byte). When a packet passes the baseband filtering (preamble and delimiter), it goes into RXMAC. The RXMAC performs several levels of packet filtering. Default mode is address-recognition mode, which can filter those packets not being sent to this device and/or others conforming to IEEE 802.15.4-2006 Section 7.5.6.2 specifications.

The 3-bit 'Frame type' field in FCF which is included in MAC header describes the type of the frame. There are total 8 types of frame in IEEE 802.15.4. Each bit of LREG0x23C correlated to the 8 types. When correlated bit is '1', RXMAC receives the type of packet without filtering out. When a received packet passes the filters discussed above and has the correct FCS, an 'RXOK interrupt' is issued at SREG0x31[3]. The MCU host can read the whole packet inside the RXFIFO. The RXFIFO is flushed when the length field of RXFIFFO and the last byte of the received packet are read or the host triggers a 'RX flush' at SREG0x0D[0].

Typical operation steps of RXFIFOs are available in Section 4.5.

Security FIFO

Security FIFO holds the corresponding key of each FIFO. The address mapping is as below:

Address	Description
0x280 ~ 0x28F	TX Normal FIFO key
0x290 ~ 0x29F	TX GTS1 FIFO key
0x2A0 ~ 0x2AF	TX GTS2/Beacon FIFO key
0x2B0 ~ 0x2BF	RX FIFO key

3.4. Power Management Block

Almost all wireless sensor network applications require low-power consumption to lengthen battery life. Typical battery-powered device is required to be operated over years without replacing its battery. The UZ2400 achieves low active current consumption of both the digital and the RF/analog circuits by controlling the supply voltage and using low-power architecture. Except Power down mode, the data in the digital registers/FIFOs are retained during the other power saving modes. The UZ2400 has five power saving modes that will be further described in Section 3.4.5.

For ultra low-power operation, Power-down mode is available which consumes around 0.1uA while the UZ2400 is powered down. All data stored in registers and FIFOs will be lost under Power-down mode. In this mode, The UZ2400 is able to wake up by an external wake-up signal.

3.4.1. Power Supply Scheme

The table below lists the recommended external bypass capacitors for each pin of the UZ2400. For the two power supply pins (pin 1 and pin 31), they need an extra bypass capacitor in parallel for the decoupling purpose while the rest of the power supply pins require only one bypass capacitor. The path length between the bypass capacitors to each pin should be made as short as possible.

Pin	Symbol	Bypass Capacitor 1	Bypass Capacitor 2
1	VDD_RF1	47 pF	10 nF
4	VDD_RF2	47 pF	
5	VDD_GR	100 nF	
10	VDD_3V	10 uF	
21	VDD_D	10 nF	
31	VDD_BG	47 pF	10 nF
32	VDD_A	47 pF	
35	VDD_PLL	47 pF	
37	VDD_CP	10 nF	
39	VDD_VCO	1 uF	

Table 4: Recommended external bypass capacitors

3.4.2. DC-DC Converter OFF Mode and DC-DC Converter ON/Bypass Mode

Two DC-DC Converter modes are designed for UZ2400. One is "DC-DC Converter OFF" and the other is "DC-DC Converter ON/Bypass". With the DC-DC Converter OFF mode, all the power pins should be directly hardwired to system supply voltage. Please refer to Section 4.1 for reference PCB design.

The DC-DC Converter ON/Bypass mode is offered because it consumes lower current. With the DC-DC Converter ON/Bypass, pin 1, 4, 21, 32, 35, 37 and 39 should be hardwired to pin 9, the DC-DC Converter output, while pin 5, 10 and 31 should be hardwired to power source directly. Under DC-DC Converter ON/Bypass mode, if the operating voltage lies between 3.6V and 2.0V, the DC-DC Converter should be turned on by setting LREG0x250[4]=1. However, if it is between 2.0V and 1.8V, the DC-DC Converter should be bypassed by setting LREG0x250[4]=0. When the DC-DC Converter is bypassed, pin 9 and 10 are shorted internally. To maintain good RF performance, when the supplied voltage is less than 2.0V, LREG0x273 shall be set to 0x9F.

For monitoring the operating voltage, please refer to Section 4.8 Battery Monitor Mechanism.

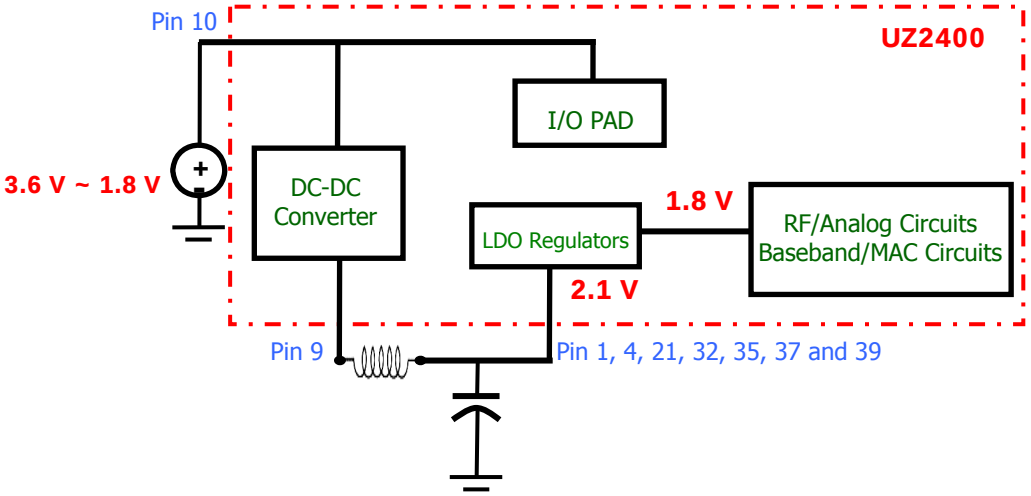


Figure 17: Block diagram of voltage regulators with DC-DC Converter ON/Bypass

For DC/DC OFF and DC/DC Bypass mode at high temperature (TA>60℃) and low voltage (2.0V>Vdd≧1.8V), the TX output power and RX sensitivity may be degraded from -3dBm and -85dBm respectively. The typical characteristics of TX output power and RX sensitivity are shown in Appendix A.

Mode	Address	Register Name	Descriptions	Value(hex)	Note
LREG	0x250	RFCTRL50	RF optimized control	07	
LREG	0x273	RFCTRL73	RF optimized control	80	Vdd=2.0V ~ 3.6V
				9F	Vdd=1.8V ~ 2.0V
LREG	0x274*	RFCTRL74	RF optimized control	E5	Vdd=2.0V ~ 3.6V
				C0	Vdd=1.8V ~ 2.0V

Table 5: Setting for DC-DC Off

Mode	Address	Register Name	Descriptions	Value(hex)	Note
LREG	0x250	RFCTRL50	RF optimized control	17	
LREG	0x273	RFCTRL73	RF optimized control	80	Vdd=2.0V ~ 3.6V
LREG	0x274	RFCTRL74	RF optimized control	C0	

Table 6: Setting for DC-DC On

Mode	Address	Register Name	Descriptions	Value(hex)	Note
LREG	0x250	RFCTRL50	RF optimized control	07	
LREG	0x273	RFCTRL73	RF optimized control	9F	Vdd=1.8V ~ 2.0V
LREG	0x274*	RFCTRL74	RF optimized control	C0	

Table 7: Setting for DC-DC Bypass

*Note. The setting of C0 at LREG0x274 results in higher output power. But the output matching may need some modification for EVM performance at low temperature.

3.4.3. Battery Monitor

The UZ2400 provides a function to monitor the system supplied voltage. A 4-bit voltage threshold can be configured so that when the supplied voltage is lower than the threshold, the system will be notified. For battery monitor function, please refer to Section 4.8.

3.4.4. Power-on Reset

The UZ2400 has a built-in power-on reset (POR) circuit which automatically resets all registers whenever the power is turned on. The 32 MHz oscillator circuit starts to make the frequency of the right clock stable after power-on. The whole process takes 3ms for clock circuit to become stable and complete the power-on reset. It is highly recommended that the user waits at least 3ms before starting to access the UZ2400.

3.4.5. Power Saving Modes

The power modes of the UZ2400 are classified into the following five modes:

- IDLE: RF circuit off. The regulator, oscillator, and digital circuits are on
- HALT: RF/MAC/BB shutdown while the system clock, output clock and the sleep clock remain active
- STANDBY: RF/MAC/BB shutdown while the sleep clock remains active
- DEEP_SLEEP: All power is shutdown except the power to the digital circuits. Register and FIFO data are retained.
- POWER_DOWN: All power is shutdown. Register and FIFO data are not retained, an external wake-up signal can wake up the UZ2400.

The only difference between STANDBY mode and DEEP SLEEP mode is the power status of the sleep clock. IDLE mode is rarely used because the device should at least always turns on its RX circuit to capture the on-air RF signals. HALT mode provides an option so that the UZ2400 can still provide the 32 MHz clock (or its dividend) through pin 26 CLK_OUT to host MCU.

The power management control is used for the low power operation of the MAC and the baseband modules. It manages to turn on and off the 32 MHz clock when the IC goes into sleep mode. By turning off the 32 MHz clock, the MAC and baseband circuits become inactive regardless whether their power supplies exist or not.

All the digital modules are clock-gated automatically. That means only when a module is functioning, its clock would then be turned on. For example, the clock of the security module is turned off if the security feature is disabled. This approach efficiently decreases a certain amount of the current consumption.

With the help of the on-chip main counter and remain counter, the UZ2400 is able to switch between ACTIVE and STANDBY modes for both Beacon mode and Non-Beacon mode. Detailed descriptions are available in Section 3.4.6. If DEEP_SLEEP mode and POWER_DOWN mode are desired instead of STANDBY mode, the MCU host has to control the time of sleep process, and Beacon-enabled mode is not suggested under this operation.

3.4.6. Counters for Power Saving Modes

As shown in Figure 18, there are two dedicated time counters in the UZ2400 for sleep mode operation. One is called main counter and the other is called remain counter. The unit of a tick differs between the two counters since the clock for main counter is driven by a sleep clock which is either internal oscillator or 32.768 kHz crystal oscillator. The remain counter is driven by the 16 MHz clock. The sleep reference interval is calculated using the combination of the two time counts of main counter and remain counter to achieve time accuracy.

Sleep Reference Interval

The sleep reference interval shown in Figure18 is composed of three parts. In the beginning, there is the front remain clock period. In the middle, there is the main clock period which is the major component of the sleep reference interval. In the end, there is the rear remain clock period which is identical to the front clock period. The front and rear remain clock periods increase the accuracy of sleep intervals.

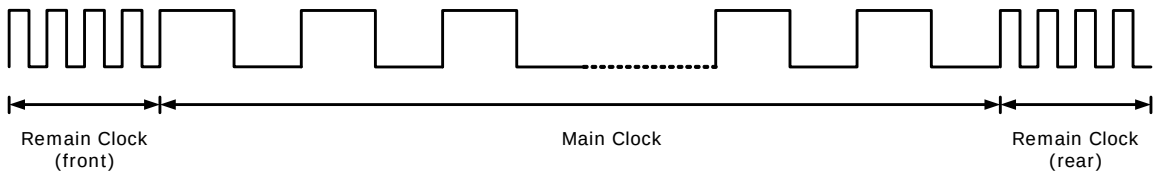


Figure 18: Composition of sleep reference interval

Sleep Alert (SLPIF, SREG0x31[7])

The sleep alert is issued by the TXMAC on the boundary between the active (composed of CAP and CFP) and the inactive period which is defined in Beacon-enabled mode in IEEE 802.15.4 standard. The sleep alert is an interrupt event which informs the MCU host that the inactive period has been started under Beacon-enabled mode. For Non-Beacon-enabled mode, a sleep alert is disabled.

Sleep Acknowledgement (SLPACK, SREG0x35[7])

For Beacon-enabled mode, the bit 7 of the short register 'SLPACK' (SREG0x35[7]) should be issued by the MCU host to initiate the sleep process. The sleep acknowledgement also turns off the PHY block.

Start Count (STARTCNT, LREG0x229[7])

For Non-Beacon-enabled mode, the bit 7 of the long register 'STARTCNT' (LREG0x229[7]) should be set to the value '1' to initiate the sleep process. The long register 'STARTCNT' also turns off the PHY block and starts the sleep reference clock under Non-Beacon-enabled mode.

Wake-up and Wake-up Alert (WAKEIF, SREG0x31[6])

The UZ2400 wakes up when the wake-time 'WAKETIME', (LREG0x222, LREG0x223) is reached. The 32 MHz oscillator is restarted after the wake-up signal asserts itself. Since the 32 MHz oscillator needs 180us to become stable, the 32 MHz clock is not enabled immediately once the 32 MHz oscillator is restarted. The 32 MHz clock will be enabled only when one WAKECNT (SREG0x35 and SREG0x36) is reached.

IEEE 802.15.4 Application Scenarios

The followings are three power saving examples demonstrating the switching between ACTIVE and STANDBY modes for typical 802.15.4 application scenarios:

- Beacon-enabled coordinator
- Beacon-enabled device
- Non-Beacon-enabled coordinator or device

For the Beacon-enabled coordinator shown in Figure 19, the sum of the periods of the main counter, the front counter, and the rear remain counters is the beacon interval. The coordinator sends beacon packets according to the interval. A sleep alert is issued by the TX_MAC to the MCU host at the end of the active period. The MCU host issues a sleep acknowledgement to initiate the sleep process. The coordinator has to prepare the beacon packet in advance. So a 'WAKETIME' is designed into the UZ2400 in order to wake it up earlier to allow the power on the 32 MHz oscillator and make it stable. When the 'WAKETIME' matches the main counter (down counter), the 32 MHz clock is enabled. Because it takes a certain period of time for the 32 MHz clock to become stable, the clock is not provided until the 'WAKECNT' is exceeded. Therefore, the 'WAKETIME' should be longer than the 'WAKECNT'. After the rear remain counter reaches its end, another beacon is transmitted and this gives rise to next 'Superframe'.

For the Beacon-enabled device shown in Figure 20, the sum of the periods of the main counter and the front and rear remain counters is the inactive period. A sleep alert is issued by the TX_MAC to the MCU host at the end of active period. The MCU host issues a sleep acknowledgement to initiate the sleep process. The device has to be ready for receiving the beacon packet in advance. So a 'WAKETIME' is designed in the UZ2400 in order to wake up earlier to allow the power on the 32 MHz oscillator and make it stable. When the 'WAKETIME' matches the main counter (down counter), the 32MHz clock is enabled. Because it takes a certain period of time for the 32 MHz clock to become stable, the clock is not provided until the 'WAKECNT' is exceeded. Therefore, the 'WAKETIME' should be longer than the 'WAKECNT'. As the rear remain counter reaches its end, a beacon should be received and this indicates a next 'Superframe'.

In Non-Beacon-enabled mode, the same idea is adopted. The only difference is that the MCU host has to set the 'STARTCNT' bit to initiate the sleep process. The sleep reference clock is started right after the 'STARTCNT' bit is set. The used wake-up process is identical in beacon mode operation. The actual sleep time is equal to 'm - n + t' as illustrated in Figure 21.

Main Counter (MAINCNT, LREG0x226, LREG0x227, LREG0x228, LREG0x229)

Main counter uses the sleep clock to count. The sleep clock can be selected by LREG0x275[4] for the 32.768 kHz crystal oscillator or the internal oscillator. An extra clock accuracy calibration should be performed when using the internal oscillator as the sleep clock. Please refer to Section 4.6.1 for detailed calibration procedures. The count is stored from the long register LREG0x226 to LREG0x229.

Remain Counter (REMCNT, LREG0x224, LREG0x225)

Remain counter uses a 16 MHz clock (divided by 32MHz clock) to count. The count is stored in the long register LREG0x224 and LREG0x225.

Waketime (WAKETIME, LREG0x222, LREG0x223)

The '***WAKETIME***' is denoted with the number 'n' in the Figure 19, Figure 20 and Figure 21. It indicates the time when the 32 MHz oscillator should wake up from the sleep status.

Wake count (WAKECNT, SREG0x35, SREG0x36)

The WAKECNT is the time count 't' in between the restart of the 32 MHz oscillator and when it becomes stable and available. It ticks according to the chosen sleep clock.

Timed wake-up is described in the above under both beacon and non-Beacon modes. However, if a user sets both main counter and remain counter to zero, the UZ2400 will not wake up unless an immediate wake-up is triggered.

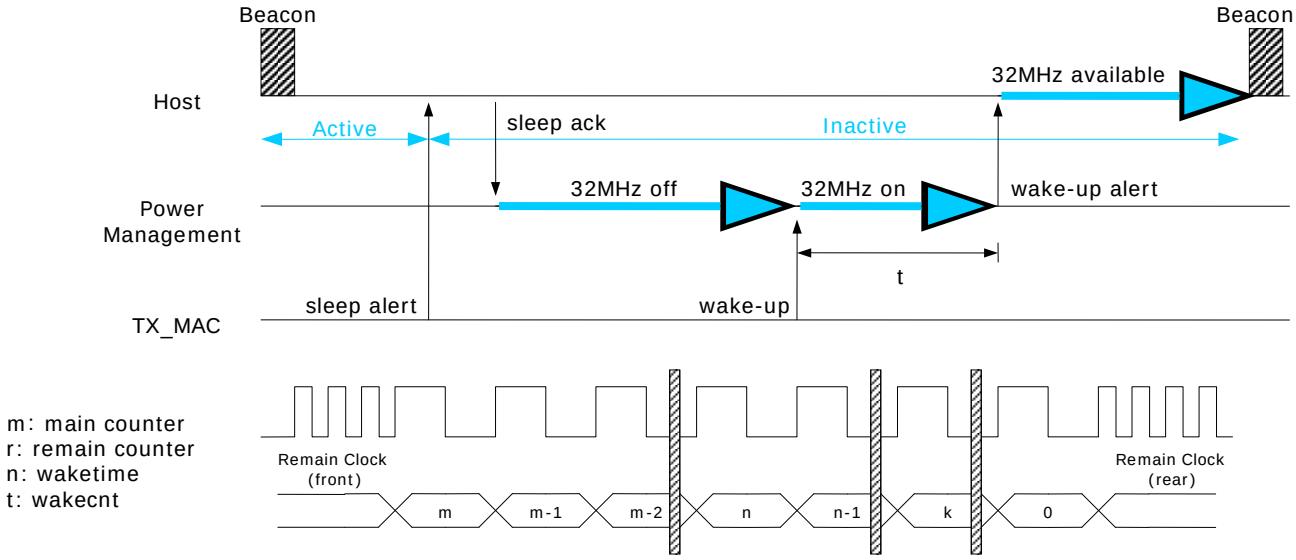


Figure 19: Sleep time diagram for the Beacon-enabled coordinator

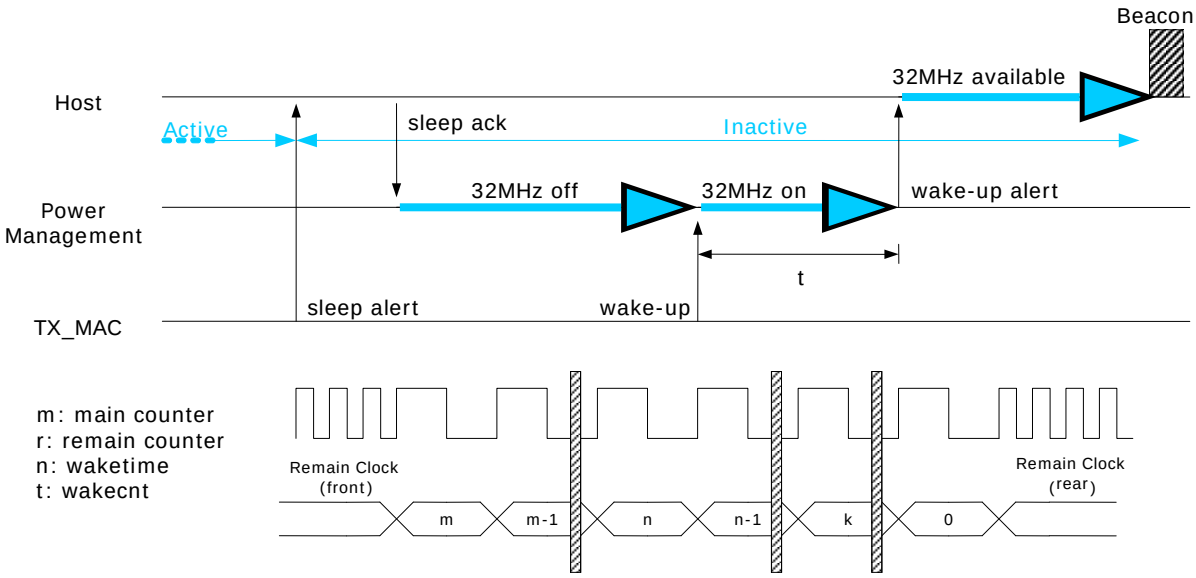


Figure 20: Sleep time diagram for the beacon-enabled device

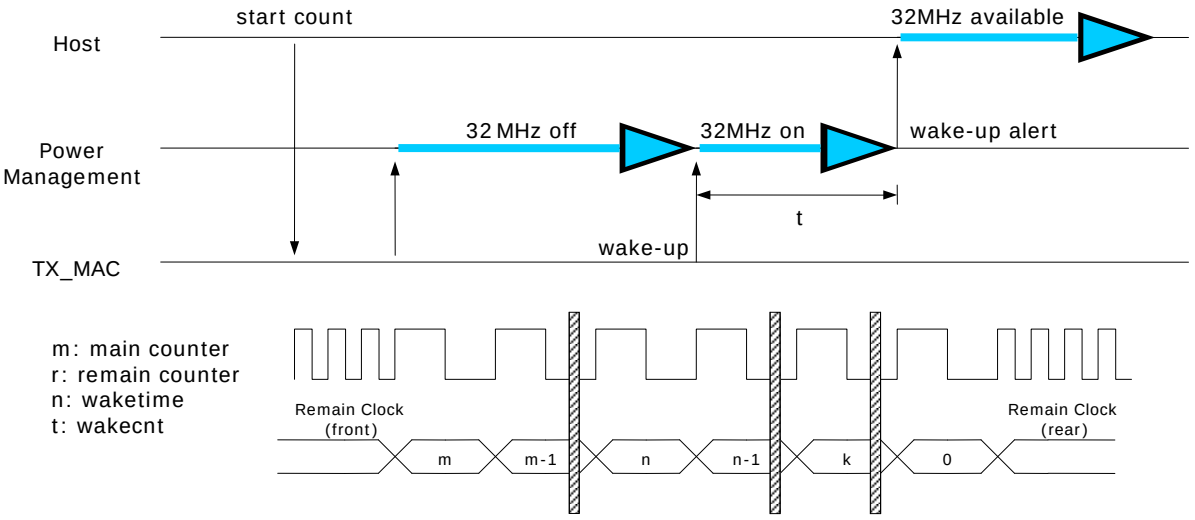
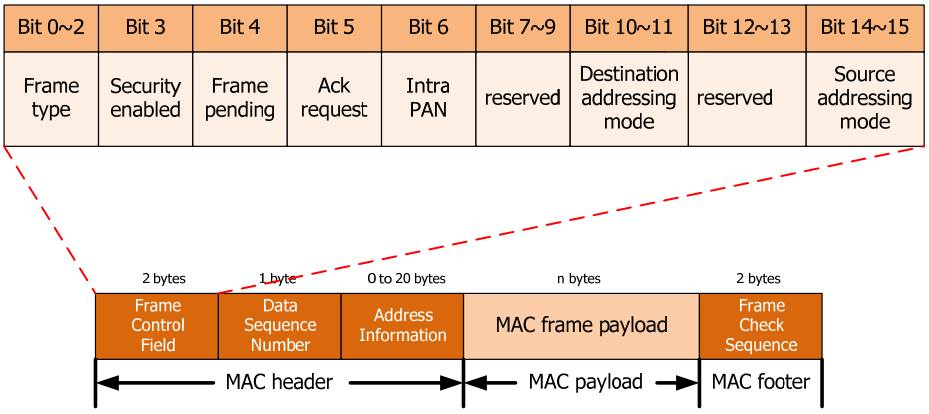


Figure 21: Sleep time diagram for Non-Beacon-enabled coordinator or device

3.4.7. Hardware Acknowledgement

Following the IEEE 802.15.4 standard, the request for the remote acknowledgement of a transmitted packet can be enabled or disabled by setting its header field. The header format is shown as below:



Bit 5 of the 'Frame control' field indicates whether the frame needs an acknowledgement or not. Users should prepare the header information correctly and write it into the TXFIFO. If the value of 'Ack request' bit-field is set to be the value'1', the receiver of this packet is required to send the ACK packet back. If the ACK frame from the remote receiver is not received, the transmitter should send the packet continually until the time period of the maximum retransmission is reached.

The UZ2400 has a built-in circuit to facilitate the acknowledgement automatically. For the transmitting side, the UZ2400 supports auto-retransmissions. For the receiving side, the UZ2400 supports auto-acknowledgements. Each of the two sides needs to set corresponding registers correctly to utilize the functions.

Auto-retransmission on TX Side

For the TXMAC to retransmit a packet automatically when an ACK is not received, SREG0x1B[2], for TX Normal FIFO, is required to set to be the value '1'. Please refer to Section 4.4.1 for more detailed description.

Auto-acknowledgement on RX Side

The RXMAC of the UZ2400 will automatically reply an ACK packet by default if 'Ack request' in the frame header is set to be the value '1'. This auto-acknowledgement feature can be disabled by setting SREG0x00[5] to '1'.

3.5. Security Engine Block

The Security module provides the security engine for the UZ2400, which is compatible to IEEE802.15.4-2006 (also adopted by ZigBee). In addition to MAC layer security requirements, the UZ2400 also provides a way called 'upper-layer security' for network or application layer use. The AES engine embedded in the UZ2400 can be used as a stand-alone co-processor, too. For more detailed information, please refer to Section 4.9.

The followings are the features of the UZ2400 Security Engine Block:

- Transmit encryption and receive decryption
- Seven modes for IEEE802.15.4-2006 of Security suites are called cipher mode listed as below.
  - AES-ENC
  - AES-ENC-MIC-128
  - AES-ENC-MIC-64
  - AES-ENC-MIC-32
  - AES-MIC-128
  - AES-MIC-64
  - AES-MIC-32
- 64 bytes Security Key FIFO is composed of four kinds of security keys. RX FIFO, Normal FIFO, and GTS1 FIFO have their own keys. The fourth kind of key is Beacon FIFO and GTS2 FIFO sharing the same key space since they will not conflict with each other.
- Security of application and network layers can be achieved using the same engine.

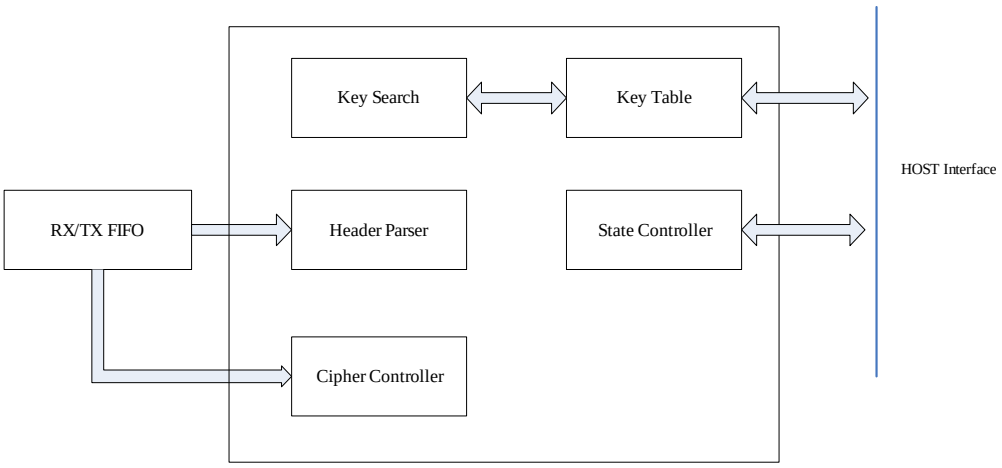


Figure 22: Security engine block diagram

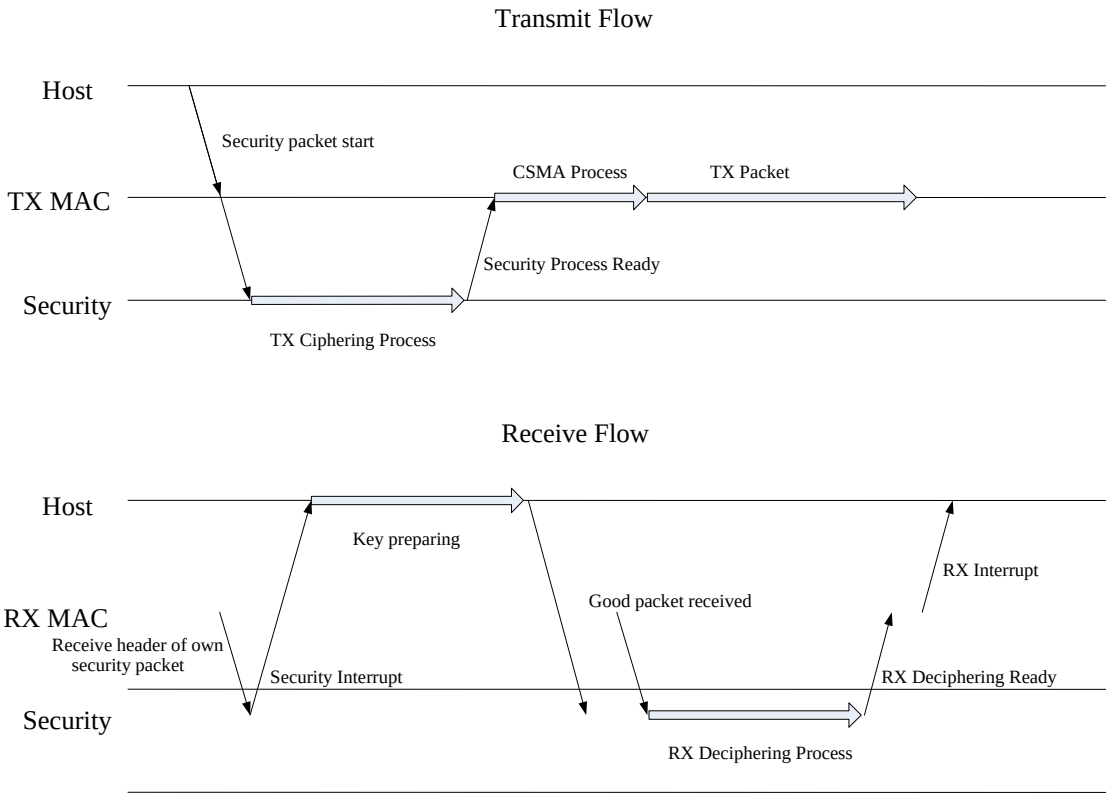


Figure 23: Security engine flow chart

3.6. Analog Circuits

3.6.1. Crystal Oscillators

The table below lists the parameters of the 32 MHz crystal oscillator used in the UZ2400. This clock is exportable at pin 26. Optional clock output frequencies are selectable among 32/16/8/4/2/1 MHz. The default clock output frequency is 1 MHz after Power-ON-Reset. This clock output can be shared with a MCU host.

User has to select 32 MHz crystal which meets the following requirements to operate the UZ2400 properly.

Parameter	Min	Typ	Max	Unit
Crystal Frequency		32		MHz
Frequency Offset	-40		40	ppm
Load Capacitance			10	pF
Recovery Time			180*	usec

Table 8: Requirements for 32 MHz crystal

* 32 MHz crystal oscillator recovery time highly depends on the shunt capacitance of 32 MHz crystal. The lower shunt capacitance value makes the recovery time shorter. This recovery time 180 usec is measured with 32 MHz crystal by NDK NX3225SA.

3.6.2. PLL Frequency Synthesizer

The loop filers of the Phase-Locked Loop (PLL) in the frequency synthesizer are integrated into the UZ2400 except one external capacitor which should be connected between pin 40 and the ground. The board layout around pin 40 should be carefully designed to avoid EMI (electro magnetic interference) in order to keep the PLL stable. The recommended value of this external capacitor is 39 pF.

3.6.3. Internal Oscillator for Sleep Clock

There is a free-running internal oscillator integrated into the UZ2400. No external component is needed for the operation of this sleep clock. User has to calibrate this sleep clock before an application starts. Please refer to Section 4.3.2 for calibration procedures.

3.6.4. 32.768 kHz Crystal Oscillator for the Sleep Clock

The table below lists the parameters of the 32.768 kHz crystal oscillator used in the UZ2400. The external 32.768 kHz crystal greatly enhances the accuracy of this oscillator so that it need not calibration any more.

Parameter	Min	Typ	Max	Unit
Crystal Frequency		32.768		kHz
Frequency Offset	-20		20	ppm
Shunt Capacitance		33		pF
Series Resistance		10		MΩ
Calibration Time		0.5		msec

Table 9: Requirement for 32.768 kHz crystal

3.7. Peripherals

3.7.1. SPI Interface

The SPI module provides slave SPI interface to read/write the control registers, FIFO and security key table of the UZ2400. The features are as below:

- A simple 4-wire SPI interface (pin 17-SO, pin 18-SI, pin 19-SCLK, and pin 20-SEN) where the UZ2400 is the slave.
- Most significant bit (MSB) of all addresses and data transfers on the SPI interface is done first.

SPI Characteristics

Parameter	Symbol	Min	Max	Units	Conditions
SCLK, clock frequency	F_{SCLK}		5	MHz	
SCLK low pulse duration	t_{CL}	100		ns	The minimum time SCLK must be low.
SCLK high pulse duration	t_{CH}	100		ns	The minimum time SCLK must be high.
SEN setup time	t_{SP}	100		ns	The minimum time SEN must be low before the first positive edge of SCLK.
SEN hold time	t_{NS}	100		ns	The minimum time SEN must be held low after the last negative edge of SCLK.
SI setup	t_{SD}	25		ns	The minimum time data must be ready at SI, before the positive edge of SCLK
SI hold time	t_{HD}	25		ns	The minimum time data must be held at SI, after the positive edge of SCLK.
Rise time	t_{RISE}		25	ns	The maximum rise time for SCLK and SEN.
Fall time	t_{FALL}		25	ns	The maximum fall time for SCLK and SEN.

Table 10: SPI characteristics

SPI Frame Format

Short Address Control Register (64 bytes)

bit [7]	bit [6:1]	bit [0]
Short Address 0	0x3F ~ 0x00	Read/Write 0 1

Long Address Control Register (128 bytes)

bit [11]	bit [10:1]	bit [0]
Long Address 1	0x27F ~ 0x200	Read/Write 0 1

Figure 24: FIFO addressing under SPI mode

SPI Time Diagrams

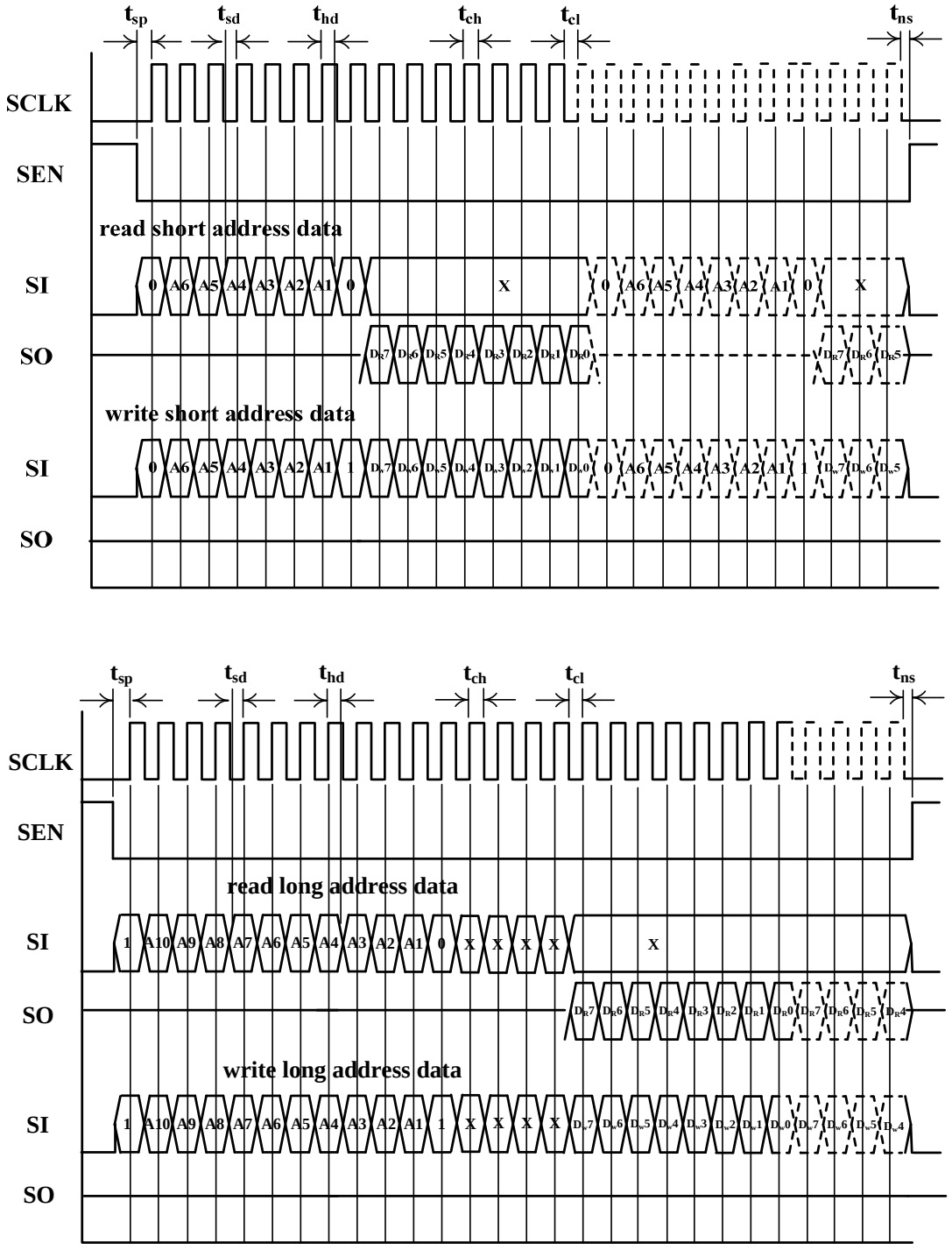


Figure 25: Time diagram and specification

Figure 25 shows the timing for the SPI short and long addressing mode respectively. SPI master will initiate a read or write operation by asserting SEN low and starting toggle SCLK and SI for the address field. The address field may be 6 or 7 bits long according to short-address or long-address mode. Followed by

the one-bit read/write indicator (0: read, 1: write) and the 8-bit write data or read data. The SEN should be high when a transaction is completed. On the SO pin, there will be an 8-bit field indicating status bits.

The SPI burst mode is provided to accelerate the FIFO access on a continuous basis. If SEN does not go high after the 8-bit write data, and the SCLK continuously toggles, the next address field will be written. Same for the read access, the data of the next address will be read. The SPI burst mode is only available for the long-address mode.

3.7.2. I²C Interface

The UZ2400 also provides I²C serial interface to access the control registers and FIFOs.

Device Operation

- CLOCK and DATA TRANSITIONS: The pin 17(SCL)/pin18 (SDA) is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.
- START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command.
- STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition.
- ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the UZ2400 in 8-bit words. The UZ2400 sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Device Addresses

The UZ2400 requires 7-bit device addresses plus control bits over the two-wire serial bus following a start condition to enable the chip for a read or write operation. The device address word consists of 11001 for the first five most significant bits as shown below. The next 2 bits are b_2 and b_1 which are selected by SCLK and SEN pins respectively. The $11001b_2b_1$ is the I²C slave address of the UZ2400. The programmable part b_2b_1 of the address is defined by hardware pins SCLK and SEN respectively. The last bit b_0 is a control bit. If b_0 is LOW, it means 'Write Operation' or else 'Read Operation'.

SCLK	SEN	Slave Address
0	0	110 0100
0	1	110 0101
1	0	110 0110
1	1	110 0111

Table 11: I²C device address configuration

Write Operations

A writing operation requires an 8-bit data word address following the slave address word and acknowledgment. Upon a receipt of this address, the UZ2400 will again respond with a zero and then clock in the first 8-bit register address. Following the receipt of the 8-bit data word, the UZ2400 will automatically output a zero and the address device, such as a microcontroller, must terminate the write sequence with a stop condition.

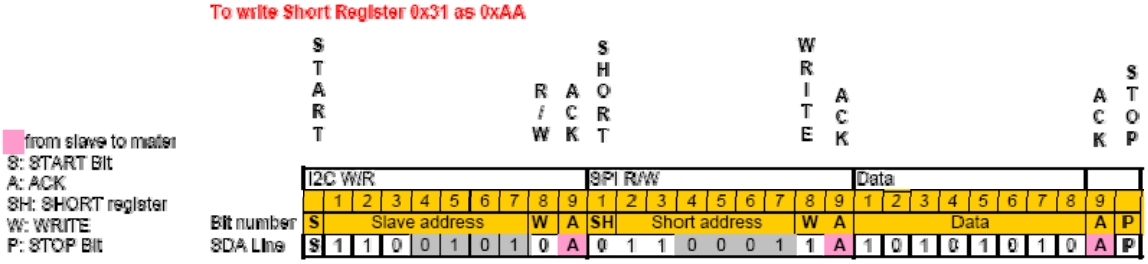
Read Operations

Read operations are initiated the same way as the write operations with the exception that the read/write select bit in the slave address word is set to one.

Once the slave address word and data word address are clocked in and acknowledged by the UZ2400, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The UZ2400 acknowledges the slave address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition

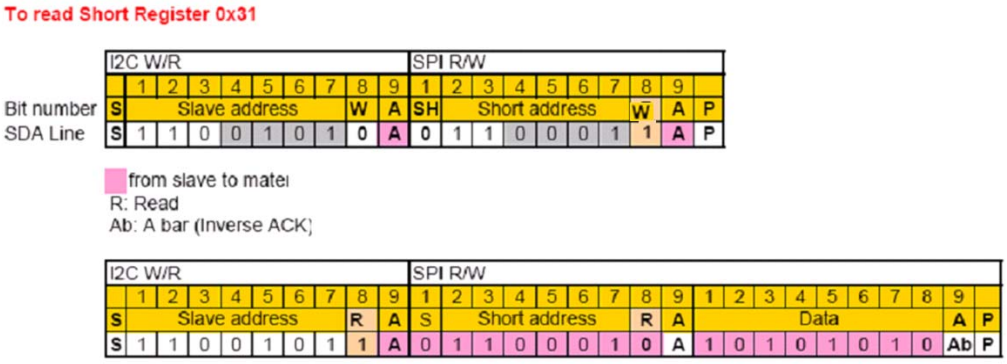
Short Register Write

Example: write short register 0x31 as 0xAA



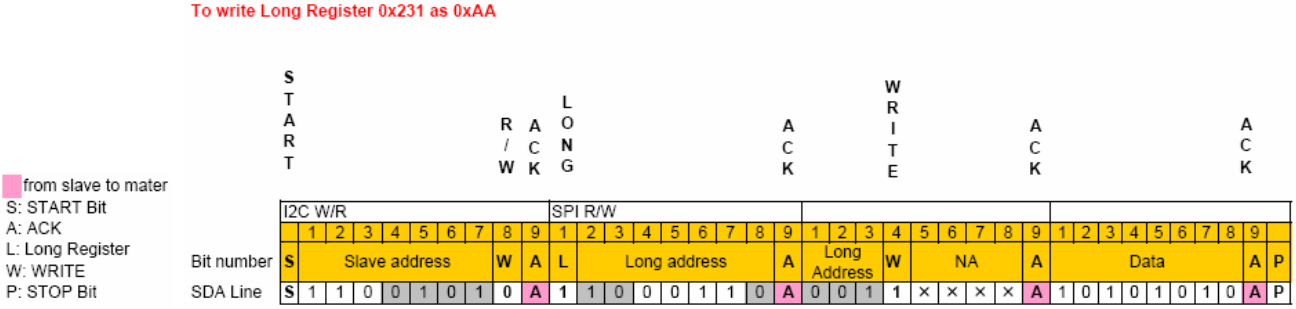
Short Register Read

Example: read short register 0x31



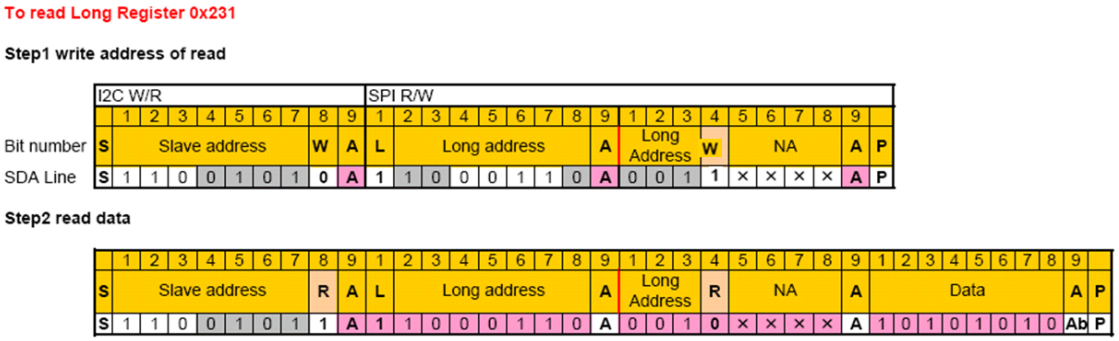
Long Register Write

Example: write long register 0x231 as 0xAA



Long Register Read

Example: read short register 0x231



3.7.3. GPIO

The UZ2400 has 4 digital GPIO pins (pin 7-GPIO0, pin 8-GPIO1, pin 11-GPIO2, and pin 12-GPIO3). Each GPIO pin can be configured as an input or an output respectively. When being configured as an output pad, the driving capability is 4mA for GPIO0 and 1mA for GPIO1, GPIO2, and GPIO3.

To benefit long range applications, GPIO0, GPIO1 and GPIO2 can be configured to control external PA and RF switch according to the current RF state automatically. Please refer to Section 4.3.5 for external PA/LNA application configuration.

3.7.4. Interrupt Signal

The UZ2400 provides an output interrupt pin (pin 16-INT) and the polarity of interrupt signal is selectable. The UZ2400 issues interrupts to the MCU host on eight possible events (For detailed interrupt event description, please see Section 4.3.4). If any event happens, the UZ2400 sets the corresponding status bit of the short register SREG0x31. If the corresponding interrupt mask in the short register SREG0x32 is clear (i.e. equals '0'), an interrupt will be issued. If it is set to '1' (masked), no interrupt will be issued, but the status is still present. An interrupt is a read-to-clear operation. Whenever SREG0x31 is read, the interrupt and the status are cleared. This is beneficial to increase the performance. The eight interrupt events are described as below:

Sleep alert interrupt (SLPIF)

In Beacon-enabled mode, the UZ2400 counts the active and inactive periods. When encountering the inactive period, the UZ2400 will issue a sleep alert interrupt to indicate the event, regardless whether it is set to be the coordinator or device mode.

Wake-up alert interrupt (WAKEIF)

Every time a wake-up event happens, the UZ2400 issues the interrupt event. This interrupt event will be issued in following scenarios:

a. When the UZ2400 is waked up from the power saving modes by register, external or timer counter except power down mode. In power down mode, the voltage regulator to the digital core is turned off. The UZ2400 will not issue the interrupt event in power down mode.

b. In using IEEE 802.15.4 slotted mode (beacon enable mode), the interrupt event is issued when the beacon frame duration expired. Please refer to the section 3.4.6. "Counters for Power Saving Modes" and the section 4.6. "Beacon Mode Operations" for the related information.

MAC timer interrupt (MACTMRIF)

The MAC timer (MACTMR), a 16 bits timer, is stored in the short registers SREG0x28 and SREG0x29. It is an internal timer ticking at MAC rate with clock period of 8us. The interrupt is issued when MACTMR down counts to '0'. Note that MACTMR does not reload.

Security interrupt (SECIF)

On receiving a packet with 'Security enable' bit set in 'Frame control' field of the packet header, a security interrupt is issued. Normally the MCU host should prepare the security key, NONCE, cipher modes or other necessary information at that moment. Then start or ignore the decryption.

Packet received interrupt (RXIF)

This interrupt is issued when an available packet is received in the RXFIFO. An available packet means that it passes an RXMAC filter, which includes a FCS check, PANID/address filtering and packet type.

GTS FIFO 1 release interrupt (TXG1IF)

This interrupt can be issued in two possible conditions. The conditions are when a packet in GTS1 FIFO is triggered and sent successfully, or when a packet is triggered and the retransmission is timed out.

GTS FIFO 2 release interrupt (TXG2IF)

This interrupt can be issued in two possible conditions. The conditions are when a packet in GTS2 FIFO is triggered and sent successfully, or when a packet is triggered and the retransmission is timed out.

TX Normal FIFO release interrupt (TXNIF)

This interrupt can be issued in two possible conditions. The conditions are when a packet in normal FIFO is triggered and sent successfully, or when a packet is triggered and the retransmission is timed out.

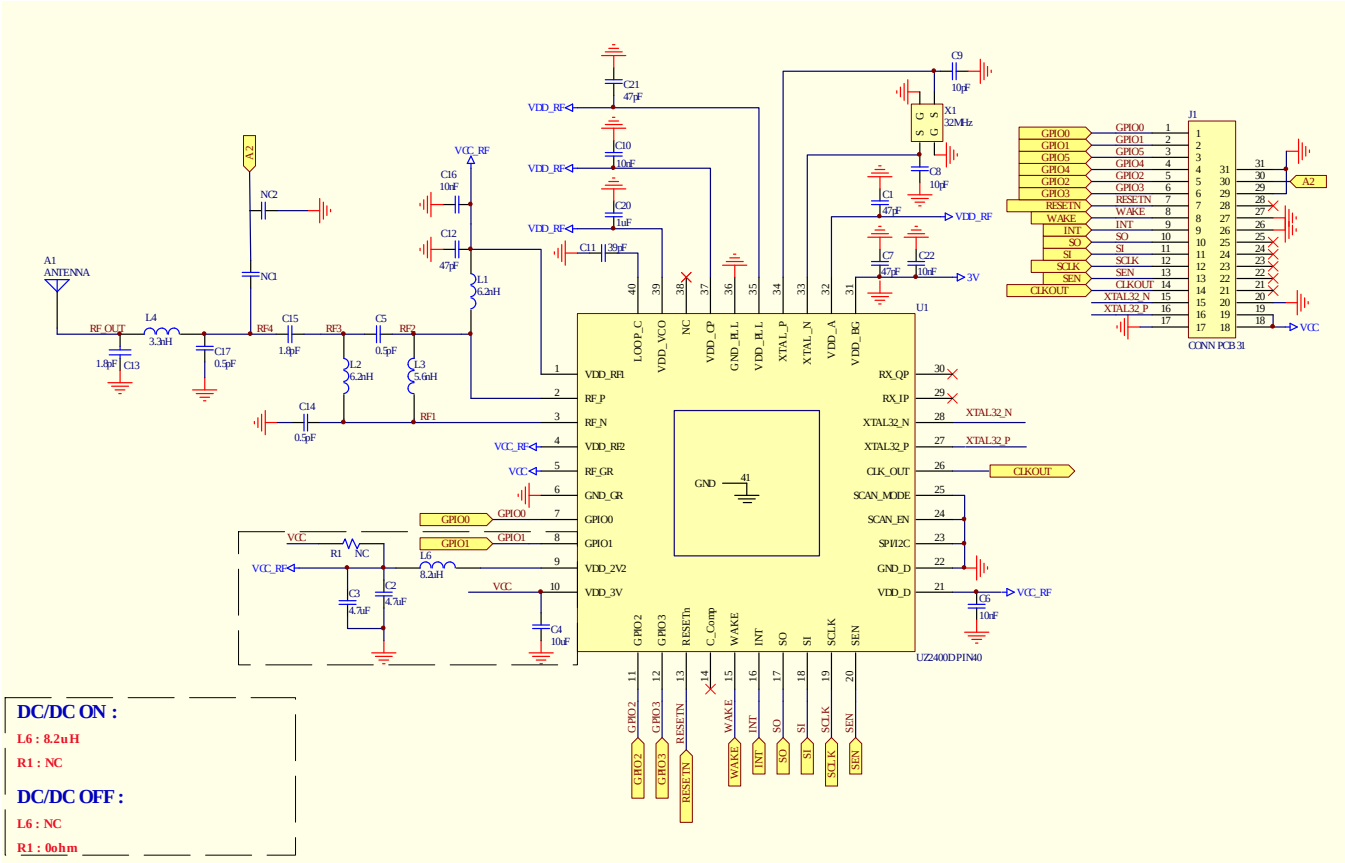
The interrupt events are indicated in the short register SREG0x31. The register is 'read-to-clear'. Each of the eight interrupts can be masked by setting the short register SREG0x32 (INTMSK).

4. Application Guide

Some typical applications are described in this chapter to help a user gain more understanding of the operation of the UZ2400.

4.1. Hardware Connection

A typical connection using the SPI interface is shown as below. The MCU host serves as a master role, and the UZ2400 serves as a slave role. The values of L1, L2, L3, C5, C14 and C15 are sensitive to PCB. And the values of L4, C13 and C17 are decided by Antenna.



* Antenna out:

▲ C17= 0.5 pF ▲ C13=1.8pF ▲L4=3.3 nH ▲ NC1, NC2: NC

(Notes: The optimal value depend on selected antenna)

* SMA out

▲L4, C13: NC▲C17=0.5 pF ▲NC1=3.6 nH ▲NC2=1.2 pF

(Notes: The optimal value depend on PCB matching)

Figure 26: Typical application circuit using SPI interface

4.2. Registers and FIFOs

The UZ2400 registers and FIFOs can be accessed by both the SPI and the I^2C interfaces. They are categorized into two kinds of address spaces. One is the short address space; the other is the long address space.

4.2.1. Memory Space

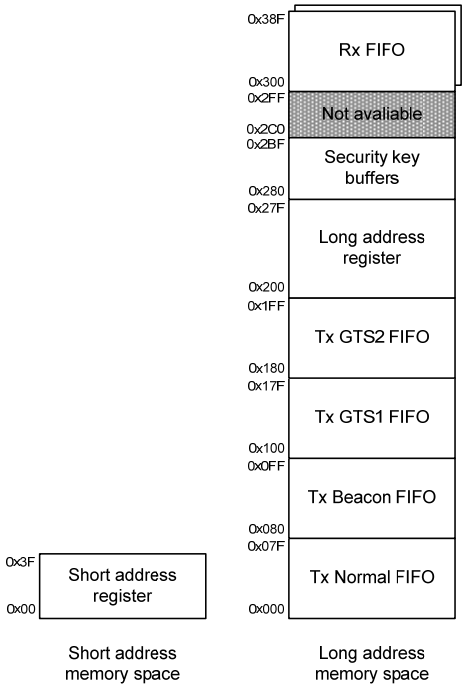


Figure 27: Memory space diagram

4.2.2. Register Summary

Short Address Registers

Legend: r=reserved

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x00	RXMCR	r	r	NOACKRSP	r	PANCOORD	COORD	r	r	0000 0000
0x01	PANIDL	PANID7	PANID6	PANID5	PANID4	PANID3	PANID2	PANID1	PANID0	0000 0000
0x02	PANIDH	PANID15	PANID14	PANID13	PANID12	PANID11	PANID10	PANID9	PANID8	0000 0000
0x03	SADRL	SADR7	SADR6	SADR5	SADR4	SADR3	SADR2	SADR1	SADR0	0000 0000
0x04	SADRH	SADR15	SADR14	SADR13	SADR12	SADR11	SADR10	SADR9	SADR8	0000 0000
0x05	EADR_0	EADR[7:0]								0000 0000
0x06	EADR_1	EADR[15:8]								0000 0000
0x07	EADR_2	EADR[23:16]								0000 0000
0x08	EADR_3	EADR[31:24]								0000 0000
0x09	EADR_4	EADR[39:32]								0000 0000
0x0A	EADR_5	EADR[47:40]								0000 0000
0x0B	EADR_6	EADR[55:48]								0000 0000
0x0C	EADR_7	EADR[63:56]								0000 0000

0x0D	RXFLUSH	r	WAKEPOL	WAKEPAD	r	NOCSMATXN	r	r	RXFLUSH	0110 0000
0x10	ORDER	BO3	BO2	BO1	BO0	SO3	SO2	SO1	SO0	1111 1111
0x11	TXMCR	NOCSMAG	r	SLOTTED	MACMINBE1	MACMINBE0	CSMABF2	CSMABF1	CSMABF0	0001 1100
0x13	ESLOTG1C	GTS1-3	GTS1-2	GTS1-1	GTS1-0	CAP3	CAP2	CAP1	CAP0	0000 0000
0x15	TXCON	TXONT6	TXONT5	TXONT4	TXONT3	TXONT2	TXONT1	TXONT0	r	0101 0001
0x16	PACON0	PACONT7	PACONT6	PACONT5	PACONT4	PACONT3	PACONT2	PACONT1	PACONT0	0010 1001
0x17	PACON1	r	r	r	PAONTS3	PAONTS2	PAONTS1	PAONTS0	PACONT8	0000 0010
0x18	FIFOEN	FIFOEN	r	TXONTS3	TXONTS2	TXONTS1	TXONTS0	TXONT8	TXONT7	1000 1000
0x1A	TXBTRIG	r	r	r	r	r	r	TXBCNSECEN	TXBCNTRIG	0000 0000
0x1B	TXNTRIG	r	r	r	PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG	0000 0000
0x1C	TXG1TRIG	TXG1IFETRY1	TXG1IFETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG	0000 0000
0x1D	TXG2TRIG	TXG2IFETRY1	TXG2IFETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG	0000 0000
0x1E	ESLOTG23	GTS3-3	GTS3-2	GTS3-1	GTS3-0	GTS2-3	GTS2-2	GTS2-1	GTS2-0	0000 0000
0x1F	ESLOTG45	GTS5-3	GTS5-2	GTS5-1	GTS5-0	GTS4-3	GTS4-2	GTS4-1	GTS4-0	0000 0000
0x20	ESLOTG6	r	r	r	r	GTS6-3	GTS6-2	GTS6-1	GTS6-0	0000 0000
0x21	TXPEND	r	r	r	r	r	r	GTSSWITCH	r	1000 0100
0x22	WAKECTL	IMMWAKE	REGWAKE	INTL5	INTL4	INTL3	INTL2	INTL1	INTL0	0000 0000
0x23	ALIGNOFF	AOFFSET7	AOFFSET6	AOFFSET5	AOFFSET4	AOFFSET3	AOFFSET2	AOFFSET1	AOFFSET0	0000 0000
0x24	TXSR	TXRETRY1	TXRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS	0000 0000
0x25	TXBCNMSK	TXBCNMSK	r	r	r	r	r	r	r	0011 0000
0x26	GATECLK	r	r	SPISYNC	ENRXM	ENGTS	ENTXM	r	r	0000 0000
0x28	MACTMRL	MACTMR7	MACTMR6	MACTMR5	MACTMR4	MACTMR3	MACTMR2	MACTMR1	MACTMR0	0000 0000
0x29	MACTMRH	MACTMR15	MACTMR14	MACTMR13	MACTMR12	MACTMR11	MACTMR10	MACTMR9	MACTMR8	0000 0000
0x2A	SOFTRST	r	r	r	r	r	RSTPWR	RSTBB	RSTMAC	0000 0000
0x2C	SECCR0	SECIGNORE	SECSTART	RXCIPHER2	RXCIPHER1	RXCIPHER0	TXNCIPHER2	TXNCIPHER1	TXNCIPHER0	0000 0000
0x2D	SECCR1	r	TXBCIPHER2	TXBCIPHER1	TXBCIPHER0	MACTMRFR	r	DISDEC	DISENC	0000 0000
0x2E	TXPEMISP	TXPET3	TXPET2	TXPET1	TXPET0	MISP3	MISP2	MISP1	MISP0	0111 0101
0x30	RXSR	RXFFFULL	WRFF1	UPSECERR	RXFFOVFL	RXCRCERR	SECDECERR	r	r	0000 0000
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000
0x32	INTMSK	SLPMSK	WAKEMSK	MACTMRMSK	SECMSK	RXMSK	TXG2MSK	TXG1MSK	TXNMSK	1111 1111
0x33	LRXSR	r	r	r	r	LRXCRCERR	r	r	r	0000 0000
0x34	SPIRXF	r	r	BATIND	r	r	r	RDFF1	RXFIFO2	0000 0000
0x35	SLPACK	SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0	0000 0000
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE	0000 0000
0x37	SECCR2	UPDEC	UPENC	TXG2CIPHER 2	TXG2CIPHER 1	TXG2CIPHER 0	TXG1CIPHER 2	TXG1CIPHER 1	TXG1CIPHER 0	0000 0000
0x38	BBREG0	PRECNT3	PRECNT2	PRECNT1	PRECNT0	r	CONT_TX	TURBO1	TURBO0	1000 0000
0x3A	BBREG2	CCAMODE1	CCAMODE0	CCATH3	CCATH2	CCATH1	CCATH0	r	r	0111 1111
0x3B	BBREG3	PREVALIDTH 3	PREVALIDTH 2	PREVALIDTH 1	PREVALIDTH 0	PREDETTH3	PREDETTH2	PREDETTH1	PREDETTH0	1101 1000
0x3C	BBREG4	CSTH3	CSTH2	CSTH1	PRECNT2	PRECNT1	PRECNT0	TXDACEDGE	RXADCEDGE	1001 1100
0x3D	BBREG5	PEAKLATE4	PEAKLATE3	PEAKLATE2	PEAKLATE1	PEAKLATE0	PEAKEARLY2	PEAKEARLY1	PEAKEARLY0	0011 1011
0x3E	BBREG6	RSSIMODE1	RSSIMODE2	RSSIMAXL	r	r	r	r	RSSIRDY	0000 0001
0x3F	BBREG7	CCAEDTH7	CCAEDTH6	CCAEDTH5	CCAEDTH4	CCAEDTH3	CCAEDTH2	CCAEDTH1	CCAEDTH0	0110 0000

Table 12: Short address register list

Long Address Registers Legend: r=reserved

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x200	RFCTRL0	CHANNEL3	CHANNEL2	CHANNEL1	CHANNEL0	r	r	PSCTRL1	PSCTRL0	0000 0001
0x201	RFCTRL1	r	r	r	r	r	r	VCORX1	VCORX0	0000 0001
0x202	RFCTRL2	r	RXFC0-1	RXFC0-0	r	r	RSSIBA2	RSSIBA1	RSSIBA0	1000 0100
0x203	RFCTRL3	TXGB4	TXGB3	TXGB2	TXGB1	TXGB0	r	r	r	0000 0000
0x204	RFCTRL4	RXFBW4	RXFBW3	RXFBW2	RXFBW1	RXFBW0	RXFCO	RXD2O1	RXD2O0	0000 0000
0x205	RFCTRL5	BATTH3	BATTH2	BATTH1	BATTH0	r	r	r	r	0000 0000
0x206	RFCTRL6	TXFBW1	TXFBW0	32MXCO1	32MCCO0	BATEN	r	r	r	1111 0000
0x207	RFCTRL7	OUTCLK2	OUTCLK1	OUTCLK0	RXFC2	TXFS1	TXFS0	r	r	0000 0000
0x208	RFCTRL8	TXD2CO1	TXD2CO0	r	r	r	r	r	r	0000 1100
0x209	SLPCAL_0	SLPCAL7	SLPCAL6	SLPCAL5	SLPCAL4	SLPCAL3	SLPCAL2	SLPCAL1	SLPCAL0	0000 0000
0x20A	SLPCAL_1	SLPCAL15	SLPCAL14	SLPCAL13	SLPCAL12	SLPCAL11	SLPCAL10	SLPCAL9	SLPCAL8	0000 0000
0x20B	SLPCAL_2	SLPCALRDY	r	r	SLPCALEN	SLPCAL19	SLPCAL18	SLPCAL17	SLPCAL16	0000 0000
0x210	RSSI	RSSI7	RSSI6	RSSI5	RSSI4	RSSI3	RSSI2	RSSI1	RSSI0	0000 0000
0x211	IRQCTRL	r	r	r	r	r	r	IRQPOL	r	0000 0000
0x212	SADRCTRL	r	r	r	r	r	r	SADRMODE1	SADRMODE0	0000 0000
0x213	SRCADR_0	SRCADR7	SRCADR6	SRCADR5	SRCADR4	SRCADR3	SRCADR2	SRCADR1	SRCADR0	0000 0000
0x214	SRCADR_1	SRCADR15	SRCADR14	SRCADR13	SRCADR12	SRCADR11	SRCADR10	SRCADR9	SRCADR8	0000 0000
0x215	SRCADR_2	SRCADR23	SRCADR22	SRCADR21	SRCADR20	SRCADR19	SRCADR18	SRCADR17	SRCADR16	0000 0000
0x216	SRCADR_3	SRCADR31	SRCADR30	SRCADR29	SRCADR28	SRCADR27	SRCADR26	SRCADR25	SRCADR24	0000 0000
0x217	SRCADR_4	SRCADR39	SRCADR38	SRCADR37	SRCADR36	SRCADR35	SRCADR34	SRCADR33	SRCADR32	0000 0000
0x218	SRCADR_5	SRCADR47	SRCADR46	SRCADR45	SRCADR44	SRCADR43	SRCADR42	SRCADR41	SRCADR40	0000 0000
0x219	SRCADR_6	SRCADR55	SRCADR54	SRCADR53	SRCADR52	SRCADR51	SRCADR50	SRCADR49	SRCADR48	0000 0000
0x21A	SRCADR_7	SRCADR63	SRCADR62	SRCADR61	SRCADR60	SRCADR59	SRCADR58	SRCADR57	SRCADR56	0000 0000
0x21E	HLEN	r	r	HLEN5	HLEN4	HLEN3	HLEN2	HLEN1	HLEN0	0000 0000
0x220	SLPCTRL	r	r	r	SCLKDIV4	SCLKDIV3	SCLKDIV2	SCLKDIV1	SCLKDIV0	0000 0000
0x222	WAKETIMEL	WAKETIME7	WAKETIME6	WAKETIME5	WAKETIME4	WAKETIME3	WAKETIME2	WAKETIME1	WAKETIME0	0000 1010
0x223	WAKETIMEH	r	r	r	r	r	WAKETIME10	WAKETIME9	WAKETIME8	0000 0000
0x224	REMCNTL	REMCNT7	REMCNT6	REMCNT5	REMCNT4	REMCNT3	REMCNT2	REMCNT1	REMCNT0	0000 0000
0x225	REMCNTH	REMCNT15	REMCNT14	REMCNT13	REMCNT12	REMCNT11	REMCNT10	REMCNT9	REMCNT8	0000 0000
0x226	MAINCNT_0	MAINCNT7	MAINCNT6	MAINCNT5	MAINCNT4	MAINCNT3	MAINCNT2	MAINCNT1	MAINCNT0	0000 0000
0x227	MAINCNT_1	MAINCNT15	MAINCNT14	MAINCNT13	MAINCNT12	MAINCNT11	MAINCNT10	MAINCNT9	MAINCNT8	0000 0000
0x228	MAINCNT_2	MAINCNT23	MAINCNT22	MAINCNT21	MAINCNT20	MAINCNT19	MAINCNT18	MAINCNT17	MAINCNT16	0000 0000
0x229	MAINCNT_3	STARTCNT	r	r	r	r	r	MAINCNT25	MAINCNT24	0000 0000
0x22F	TESTMODE	MSPI	RSSIRDY1	RSSIRDY0	RSSIWAIT1	RSSIWAIT0	TESTMODE2	TESTMODE1	TESTMODE0	0010 1000
0x230	ASSOEADR_0	ASSOEADR[7:0]								0000 0000
0x231	ASSOEADR_1	ASSOEADR[15:8]								0000 0000
0x232	ASSOEADR_2	ASSOEADR[23:16]								0000 0000
0x233	ASSOEADR_3	ASSOEADR[31:24]								0000 0000
0x234	ASSOEADR_4	ASSOEADR[39:32]								0000 0000
0x235	ASSOEADR_5	ASSOEADR[47:40]								0000 0000
0x236	ASSOEADR_6	ASSOEADR[55:48]								0000 0000

0x237	ASSOEADR_7	ASSOEADR[63:56]							0000 0000
0x238	ASSOSADRL	ASSOSADR[7:0]							0000 0000
0x239	ASSOSADRH	ASSOSADR[15:8]							0000 0000
0x23C	RXFRMTYPE	RXFTYPE7	RXFTYPE6	RXFTYPE5	RXFTYPE4	RXFTYPE3	RXFTYPE2	RXFTYPE1	RXFTYPE0	0000 1011
0x23D	GPIODIR	r	r	r	r	GPIO3DIR	GPIO2DIR	GPIO1DIR	GPIO0DIR	0011 1111
0x23E	GPIO	r	r	r	r	GPIO3	GPIO2	GPIO1	GPIO0	0000 0000
0x240	UPNONCE_0	UPNONCE[7:0]							0000 0000
0x241	UPNONCE_1	UPNONCE[15:8]							0000 0000
0x242	UPNONCE_2	UPNONCE[23:16]							0000 0000
0x243	UPNONCE_3	UPNONCE[31:24]							0000 0000
0x244	UPNONCE_4	UPNONCE[39:32]							0000 0000
0x245	UPNONCE_5	UPNONCE[47:40]							0000 0000
0x246	UPNONCE_6	UPNONCE[55:48]							0000 0000
0x247	UPNONCE_7	UPNONCE[63:56]							0000 0000
0x248	UPNONCE_8	UPNONCE[71:64]							0000 0000
0x249	UPNONCE_9	UPNONCE[79:72]							0000 0000
0x24A	UPNONCE_10	UPNONCE[81:80]							0000 0000
0x24B	UPNONCE_11	UPNONCE[95:88]							0000 0000
0x24C	UPNONCE_12	UPNONCE[89:96]							0000 0000
0x24D	SECCTRL	r	r	SEC_2006	USRFLAG	r	r	r	r	0000 0000
0x24E	ENCFLG	ENCFLG7	ENCFLG6	ENCFLG5	ENCFLG4	ENCFLG3	ENCFLG2	ENCFLG1	ENCFLG0	0000 0000
0x24F	AUTFLG	AUTFLG7	AUTFLG6	AUTFLG5	AUTFLG4	AUTFLG3	AUTFLG2	AUTFLG1	AUTFLG0	0000 0000
0x250	RFCTRL50	r	r	r	DCPOC	DCOPC3	DCOPC2	DCOPC1	DCOPC0	0000 0000
0x251	RFCTRL51	DCOPC5	DCOPC4	r	r	r	r	r	r	0000 0000
0x252	RFCTRL52	SLCTRL6	SLCTRL5	SLCTRL4	SLCTRL3	SLCTRL2	SLCTRL1	SLCTRL0	32MXCTRL	1111 1111
0x253	RFCTRL53	r	FIFOPS	DIGITALPS	r	PA1CFEN	PA1CTRLF-2	PA1CTRLF-1	PA1CTRLF-0	0000 0000
0x254	RFCTRL54	1MCSEN	1MFRCH6	1MCSCH5	1MCSCH4	1MCSCH3	1MCSCH2	1MCSCH1	1MCSCH0	0000 0000
0x255	RFCTRL55	r	r	HALTCTRL	r	r	r	r	r	0000 0000
0x259	RFCTRL59	r	r	r	r	r	r	r	PLLOPT4	0000 0001
0x273	RFCTRL73	VCOTXOPT1	VCOTXOPT0	r	ADCOPT	PLLOPT3	PLLOPT2	PLLOPT1	PLLOPT0	0000 0000
0x274	RFCTRL74	PA1CCEN	PA1CTRLC-2	PA1CTRLC-1	PA1CTRLC-0	PA2CTRL-3	PA2CTRL-2	PA2CTRL-1	PA2CTRL-0	1100 1010
0x275	RFCTRL75	r	r	r	SCLKSEL	SCLKOPT3	SCLKOPT2	SCLKOPT1	SCLKOPT0	0001 0101
0x276	RFCTRL76	r	r	r	r	r	SCLKOPT6	SCLKOPT5	SCLKOPT4	0000 0001
0x277	RFCTRL77	r	r	SLPSEL1	SLPSEL0	SLPVCTRL1	SLPVCTRL0	SLPVSEL1	SLPVSEL0	0000 1000
0x27A	INITCNTL	INITCNT7	INITCNT6	INITCNT5	INITCNT4	INITCNT3	INITCNT2	INITCNT1	INITCNT0	0000 0000
0x27B	INITCNTH	INITCNT15	INITCNT14	INITCNT13	INITCNT12	INITCNT11	INITCNT10	INITCNT9	INITCNT8	0000 0000

Table 13: Long address register list

4.2.3. Security Key FIFO

A security key FIFO stores the security keys, which are needed for the secured data packet transferring.

Address	Description
0x280 ~ 0x28F	TX Normal FIFO key
0x290 ~ 0x29F	GTS1 FIFO key
0x2A0 ~ 0x2AF	GTS2/Beacon FIFO key
0x2B0 ~ 0x2BF	RX FIFO key

Table 14: Security key FIFO mapping

4.3. Basic Operations

4.3.1. Initialization

Mode	Address	Register Name	Descriptions	Value (hex)	Note
SREG	0x26	GATECLK	Enable SPI sync function	20	
SREG	0x17	PACON1	Increase PAON time	08	
SREG	0x18	FIFOEN	Increase TXON time	94	
SREG	0x2E	TXPEMISP	VCO calibration period	95	
SREG	0x3B	BBREG3	Preamble Search Energy Detection	50	
SREG	0x3D	BBREG5	Preamble Searching Time	07	
SREG	0x3E	BBREG6	Append RSSI value in RX packets	40	
LREG	0x200	RFCTRL0	RF optimized control	03	
LREG	0x201	RFCTRL1	RF optimized control	01	
LREG	0x202	RFCTRL2	RF optimized control	74	
LREG	0x204	RFCTRL4	RF optimized control	06	
LREG	0x206[*1]	RFCTRL6	RF optimized control	10	250K bps
LREG	0x207[*1]	RFCTRL7	RF optimized control	EC	250K bps
LREG	0x208	RFCTRL8	RF optimized control	8C	
LREG	0x23D	GPIODIR	For Setting GPIO to Output	00	
LREG	0x24D	SECCTRL	Enable IEEE802.15.4-2006 security	20	
LREG	0x250[*2]	RFCTRL50	RF optimized control	07	DC-DC OFF
LREG	0x251	RFCTRL51	RF optimized control	C0	
LREG	0x252	RFCTRL52	RF optimized control	01	
LREG	0x259	RFCTRL59	RF optimized control	00	
LREG	0x273[*2]	RFCTRL73	RF optimized control	80	DC-DC OFF Vdd=2.0V ~ 3.6V
LREG	0x274[*2]	RFCTRL74	RF optimized control	E5	DC-DC OFF Vdd=2.0V ~ 3.6V
LREG	0x275	RFCTRL75	RF optimized control	13	
LREG	0x276	RFCTRL76	RF optimized control	07	
SREG	0x32	INTMSK	Enable all interrupt	00	
SREG	0x2A	SOFTRST	Baseband Reset	02	

SREG	0x36	RFCTL	Hold RF state machine in Reset	04	
SREG	0x36	RFCTL	Normal operation	00	
SREG	0x36	RFCTL	Force to TX mode	02	
Wait for 192 us					
SREG	0x36	RFCTL	Force to RX mode	01	
Wait for 192 us					
SREG	0x36	RFCTL	Normal operation	00	
SREG	0x35	SLPACK	32MHz clock recovery time		Ref 4.3.2.

The initialization procedure mentioned above is valid for most of the application conditions.

Note 1: Please refer to Section 4.3.6 for turbo mode setting.
Note 2: Please refer to Section 3.4.2 for DC-DC converter OFF mode and DC-DC Converter ON/Bypass mode.

Registers Associated with Initialization

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x17	PACON1	r	r	r	PAONTS3	PAONTS2	PAONTS1	PAONTS0	PACONT8	0000 0010
0x18	FIFOEN	FIFOEN	r	TXONTS3	TXONTS2	TXONTS1	TXONTS0	TXONT8	TXONT7	1000 1000
0x26	GATECLK	r	r	SPISYNC	ENRXM	ENGTS	ENTXM	r	r	0000 0000
0x2A	SOFTRST	r	r	r	r	r	RSTPWR	RSTBB	RSTMAC	0000 0000
0x2E	TXPEMISP	TXPET3	TXPET2	TXPET1	TXPET0	MISP3	MISP2	MISP1	MISP0	0111 0101
0x32	INTMSK	SLPMSK	WAKEMSK	MACTMRMSK	SECMSK	RXMSK	TXG2MSK	TXG1MSK	TXNMSK	1111 1111
0x35	SLPACK	SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0	0000 0000
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE	0000 0000
0x3B	BBREG3	PREVALIDTH 3	PREVALIDTH 2	PREVALIDTH 1	PREVALIDTH 0	PREDETTH3	PREDETTH2	PREDETTH1	PREDETTH0	1101 1000
0x3D	BBREG5	PEAKLATE4	PEAKLATE3	PEAKLATE2	PEAKLATE1	PEAKLATE0	PEAKEARLY2	PEAKEARLY1	PEAKEARLY0	0011 1011
0x3E	BBREG6	RSSIMODE1	RSSIMODE2	RSSIMAXL	r	r	r	r	RSSIRDY	0000 0001
0x200	RFCTRL0	CHANNEL3	CHANNEL2	CHANNEL1	CHANNEL0	r	r	PSCTRL1	PSCTRL0	0000 0001
0x201	RFCTRL1	r	r	r	r	r	r	VCORX1	VCORX0	0000 0001
0x202	RFCTRL2	r	RXFC0-1	RXFC0-0	r	r	RSSIBA2	RSSIBA1	RSSIBA0	1000 0100
0x204	RFCTRL4	RXFBW4	RXFBW3	RXFBW2	RXFBW1	RXFBW0	RXFCO	RXD2O1	RXD2O0	0000 0000
0x206	RFCTRL6	TXFBW1	TXFBW0	32MXCO1	32MCCO0	BATEN	r	r	r	1111 0000
0x207	RFCTRL7	OUTCLK2	OUTCLK1	OUTCLK0	RXFC2	TXFS1	TXFS0	r	r	0000 0000
0x208	RFCTRL8	TXD2CO1	TXD2CO0	r	r	r	r	r	r	0000 1100
0x23D	GPIODIR	r	r	r	r	GPIO3DIR	GPIO2DIR	GPIO1DIR	GPIO0DIR	0011 1111
0x24D	SECCTRL	r	r	SEC_2006	USRFLAG	r	r	r	r	0000 0000
0x250	RFCTRL50	r	r	r	DCPOC	DCOPC3	DCOPC2	DCOPC1	DCOPC0	0000 0000
0x251	RFCTRL51	DCOPC5	DCOPC4	r	r	r	r	r	r	0000 0000
0x252	RFCTRL52	SLCTRL6	SLCTRL5	SLCTRL4	SLCTRL3	SLCTRL2	SLCTRL1	SLCTRL0	32MXCTRL	1111 1111
0x259	RFCTRL59	r	r	r	r	r	r	r	PLLOPT3	0000 0001
0x273	RFCTRL73	VCOTXOPT1	VCOTXOPT0	r	ADCOPT	PLLOPT3	PLLOPT2	PLLOPT1	PLLOPT0	0000 0000
0x274	RFCTRL74	PA1CCEN	PA1CTRLC-2	PA1CTRLC-1	PA1CTRLC-0	PA2CTRL-3	PA2CTRL-2	PA2CTRL-1	PA2CTRL-0	1100 1010
0x275	RFCTRL75	r	r	r	SCLKSEL	SCLKOPT3	SCLKOPT2	SCLKOPT1	SCLKOPT0	0001 0101
0x276	RFCTRL76	r	r	r	r	r	SCLKOPT6	SCLKOPT5	SCLKOPT4	0000 0001

4.3.2. Clock Recovery Time

WAKECNT is used for the internal sleep clock of the UZ2400 to recover from sleep mode.
WAKECNT = {SREG0x36[4:3], SREG0x35[6:0]}

Step 1.

Calibrate the sleep clock frequency:

- The UZ2400 uses a 16 MHz system clock to calibrate the sleep clock frequency. To do the calibration, set LREG0x20B[4] to '1', and then keep polling LREG0x20B until the value of LREG0x20B[7] becomes '1'. After the value of LREG0x20B[7] becomes '1', LREG0x20B[3:0], LREG0x20A, LREG0x209 form a 20-bit value C. Then the period of the sleep clock (Psleepclock) can be calculated by the following equation:

$$P_{sleepclock} = \frac{62.5 \times C}{16}(ns)$$

- If the sleep clock frequency is higher than the expected value, users can configure LREG0x220[4:0] to slow the clock rate. The new clock period $P_{sleepclock\_new}$ is obtained by the following equation:

$$P_{sleepclock\_new} = P_{sleepclock\_ori} \times 2^{LREG0x220[4:0]}$$

Step 2.

Configure the recovery time of 32 MHz clock by setting WAKECNT to 180 us.

{SREG0x36[4:3], SREG0x35[6:0]} = (1000*180 us) /Psleepclock

For example, the period of the sleep clock (Psleepclock) is 10000 ns.
The WAKECNT = 180*1000/10000 = 18 (0x12).

Step 3.

The detailed WAKECNT setting of each power saving mode

HALT Mode:

Because the system clock remains active, the HALT mode does not need system clock recovery time. Set WAKECNT to minimum value 0x01

STANDBY Mode:

(1) Wake-up by Register Trigger
Please set WAKECNT to 0x12

(2) WAKE Pin Wake-up
To use this approach to wake up, UZ2400 will have to take 6 sleep clock periods to synchronize the wake-up circuits first. The WAKECNT will start to count down only when the synchronization is achieved. Thus the total clock recovery time in this case is (6 plus the WAKECNT count) times the sleep clock period. That means in order to keep the specified 180 µsec total clock recovery time, the user has to reduce the WAKECNT count by 6 as shown in the instruction below. However in no case the value of WAKECNT shall be reduced to less than 1.

For example, the period of the sleep clock (Psleepclock) is 10000 ns.
WAKECNT = 180*1000/10000 - 6 = 12 (0x0C).

If a clock divisor is used:
When LREG0x220[4:0] = 1, WAKECNT = New WAKECNT – 0x06/2
When LREG0x220[4:0] = 2, WAKECNT = New WAKECNT – 0x06/4
When LREG0x220[4:0] is more than 3, WAKECNT = New WAKECNT

DEEP SLEEP Mode:

Please set WAKECNT to 0x12

Registers Associated with Clock Recovery Time

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x35	SLPACK	SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0	0000 0000
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE	0000 0000
0x209	SLPCAL_0	SLPCAL7	SLPCAL6	SLPCAL5	SLPCAL4	SLPCAL3	SLPCAL2	SLPCAL1	SLPCAL0	0000 0000
0x20A	SLPCAL_1	SLPCAL15	SLPCAL14	SLPCAL13	SLPCAL12	SLPCAL11	SLPCAL10	SLPCAL9	SLPCAL8	0000 0000
0x20B	SLPCAL_2	SLPCALRDY	r	r	SLPCALEN	SLPCAL19	SLPCAL18	SLPCAL17	SLPCAL16	0000 0000
0x220	SLPCTRL	r	r	r	SCLKDIV4	SCLKDIV3	SCLKDIV2	SCLKDIV1	SCLKDIV0	0000 0000

4.3.3. Change Channel Procedure

Step 1.

Set RF operation channel. UZ2400 operates in 2.4 GHz ISM band. The operating frequency is divided into 16 channels. User can select one of the channels by configuring LREG0x200.

Step 2.

Turn on the TX MAC gated clock by setting SREG0x26[2] to '1'. To avoid an incomplete acknowledgment frame transmission happen during RF state machine reset period.

Step 3.

After the operation channel is set, RF state machine should be reset by the following settings.

Mode	Address	Register Name	Descriptions	Value(hex)	Note
SREG	0x36	RFCTL	Force to TX mode	02	
Wait for 192 us					
SREG	0x36	RFCTL	Force to RX mode	01	
Wait for 192 us					
SREG	0x36	RFCTL	Normal operation	00	

Step 4.

After RF reset, delay for a while to ensure the acknowledgment frame, if any, is successfully transmitted.

2Mbps mode: delay 250 s
1Mbps mode: delay 300 s
250kbps mode: delay 550 s

Step 5.
To disable the TX MAC gated clock by setting SREG26[2] to '0'.

Registers Associated with Change Channel Procedure

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x26	GATECLK	r	r	SPISYNC	ENRXM	ENGTS	ENTXM	r	r	0000 0000
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE	0000 0000
0x200	RFCTRL0	CHANNEL3	CHANNEL2	CHANNEL1	CHANNEL0	r	r	PSCTRL1	PSCTRL0	0000 0001

4.3.4. Interrupt Configuration

The UZ2400 issues a hardware interrupt via pin 16 to the MCU host. Two registers need to be set correctly with respect to a user's application. The interrupt status can be read from SREG0x31. The interrupt is by default sent to the MCU host as a falling edge signal after mask removed. The interrupt should be configured in the step 2 of the initialization procedure by setting SREG0x32. All the interrupts are masked (disabled) by default.

Registers Associated with Interrupt Configuration

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000
0x32	INTMSK	SLPMSK	WAKEMSK	MACTMRMSK	SECMSK	RXMSK	TXG2MSK	TXG1MSK	TXNMSK	1111 1111
0x211	IRQCTRL	r	r	r	r	r	r	IRQPOL	r	0000 0000

4.3.5. External Power Amplifier Configuration

Set LREG0x22F[2:0] to '001' to enable the PA function. This register setting integrates the PA enable and the RF Switch Control (TX branch, RX branch) by utilizing pin GPIO0, pin GPIO1, and pin GPIO2. If the UZ2400 is in TX mode, the pin GPIO0 (external PA enable) and pin GPIO1 (TX branch enable) will be pulled HIGH, and the pin GPIO2 (RX branch enable) will be pulled LOW automatically. If the UZ2400 is in RX mode, the pin GPIO0 and pin GPIO1 will be pulled LOW, and the pin GPIO2 will be pulled HIGH automatically. It automatically changes the status of the external PA and the TX/RX branch corresponding to TX or RX mode of the UZ2400.

- TX mode: GPIO0 HIGH, GPIO1 HIGH, GPIO2 LOW
- RX mode: GPIO0 LOW, GPIO1 LOW, GPIO2 HIGH

Registers Associated with External Power Amplifier Configuration

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x22F	TESTMODE	MSPI	RSSIRDY1	RSSIRDY0	RSSIWAIT1	RSSIWAIT0	TESTMODE2	TESTMODE1	TESTMODE0	0010 1000

4.3.6. Turbo Mode Configuration

The UZ2400 provides 1M/2M bps Turbo modes to transmit and receive data at a higher rate compared to the standard 250kbps. That is, the data rate is 4 or 8 times faster than the standard rate. Turbo mode provide an added capability for applications which require higher data rate. The application circuit does not need any modification for Turbo modes application.

To use the UZ2400 in 250kbps, 1Mbps and 2Mbps, the following registers need to be configured as below.

Address mode	Addr	Register Name	Descriptions	Value (hex)		
				250k	1M	2M
LREG	0x206	RFCTL6	RF optimized control	0x10	0x50	0x50
LREG	0x207	RFCTL7	RF optimized control	0xEC	0xFC	0xEC
SREG	0x38	BBREG0	Enable Normal/Turbo mode	0x80	0x81	0x83
SREG	0x2A	SOFTRST	Baseband Reset	0x02		

Registers Associated with Turbo Mode Configuration

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x2A	SOFTRST	r	r	r	r	r	RSTPWR	RSTBB	RSTMAC	0000 0000
0x38	BBREG0	PRECNT3	PRECNT2	PRECNT1	PRECNT0	r	CONT_TX	TURBO1	TURBO0	1000 0000
0x206	RFCTRL6	TXFBW1	TXFBW0	32MXCO1	32MCCO0	BATEN	r	r	r	1111 0000
0x207	RFCTRL7	OUTCLK2	OUTCLK1	OUTCLK0	RXFC2	TXFS1	TXFS0	r	r	0000 0000

4.4. Typical TX Operations

The TXMAC inside the UZ2400 will automatically generate the preamble and Start-of-Frame delimiter fields when transmitting. Additionally, the TXMAC can generate any padding (if needed) and the CRC, if configured to do so. The MCU host must write all other frame fields into the buffer memory for transmission operation.

4.4.1. Transmit Packet in Normal FIFO

To send a packet in Normal FIFO, there are several steps to follow:

Step 1.

Fill in Normal FIFO with the packet to send. The format is as follows

TXFIFO Address			
0x000			2+M+N
1 Byte	1 Bytes	M Bytes	N Bytes
Header length*1	Frame length*2	Header	Payload

*1: only lower 6 bits are valid.

*2: Value range is 1-125

Table 15: Normal FIFO format

Step 2.

Set an Ackreq in SREG0x1B[2] if an acknowledgement from the receiver is required. If the Ackreq is set, the UZ2400 automatically retransmits the packet if there is no acknowledgement sent back. The UZ2400 will retransmit the packet till the number of the Max trial times specified by IEEE 802.15.4 is reached.

Step 3.

Set the trigger bit SREG0x1B[0] to send a packet. This bit will be automatically cleared. At this time, the TXMAC will perform CSMA-CA and send the packet at the right moment.

Step 4.

Wait for the interrupt status shown in SREG0x31[0].

Step 5.

Check SREG0x24[0] to see if transmission is successful. SREG0x24[0]=0 means transmission successful and the ACK was received. The number of times of the retransmission can be read at SREG0x24[7:6]. SREG0x24[0]=1 means transmission failed and ACK was not received.

Registers Associated with Transmit Packet in Normal FIFO

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x1B	TXNTRIG	r	r	r	PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG	0000 0000
0x24	TXSR	TXRETRY1	TXRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS	0000 0000
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000

4.4.2. Transmit Packet in GTS FIFO

This section describes how to trigger the GTS FIFO to send a packet. As for the setting using GTS in beacon mode, please refer to Section 4.6. To send a packet in the GTS FIFO, there are several steps to follow:

Step 1.

Fill in the GTS FIFO with a packet to send. The format is the same as Normal FIFO.

GTS1 FIFO Address 0x100			102+M+N
GTS2 FIFO Address 0x180			182+M+N
1 Byte	1 Bytes	M Bytes	N Bytes
Header length*1	Frame length*2	Header	Payload

*1: only lower 6 bits are valid.

*2: Value range is 1-125

Table 16: GTS FIFO format

Step 2.

Set an Ackreq in {SREG0x1C[2], SREG0x1D[2]} if an acknowledgement from the receiver is required. If the Ackreq is set, the UZ2400 automatically retransmits the packet if there is no acknowledgement sent back. The UZ2400 will retransmit the packet till the number of the Max trial times specified by IEEE 802.15.4 is reached or when the CFP is ended.

Step 3.

Set the corresponding GTS slot number in {SREG0x1C[5:3], SREG0x1D[5:3]} to decide when to send this packet in FIFO.

Step 4.

Set the retransmission time at SREG0x1C[7:6] and SREG0x1D[7:6] for GTS1 and GTS2 FIFO respectively.

Step 5.

Set the trigger bit {SREG0x1C[0], SREG0x1D[0]} to send the packet. This bit will be automatically cleared. At this time, the TXMAC will wait until the corresponding GTS slot sends the packet at that moment.

Step 6.

Wait for the interrupt status shown in SREG0x31[1] for GTS1 FIFO and SREG0x31[2] for GTS2 FIFO.

Step 7.

Check SREG0x24[1] or SREG0x24[2] to see if transmission is successful. SREG0x24[1]=0 or SREG0x24[2]=0 mean transmission successful and the ACK was received. The number of times of the re-transmission can be read at SREG0x1C[7:6] or SREG0x1D[7:6]. SREG0x24[1]=1 or SREG0x24[2]=1 mean transmission failed and ACK was not received.

Registers Associated with Transmit Packet in GTS FIFO

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x1C	TXG1TRIG	TXG1IFETRY1	TXG1IFETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG	0000 0000
0x1D	TXG2TRIG	TXG2IFETRY1	TXG2IFETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG	0000 0000
0x24	TXSR	TXRETRY1	TXRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS	0000 0000
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000

4.4.3. Transmit Packet with Security Encryption

To send a secured packet TXFIFO, there are several steps to follow:

Step 1.

Load the header length (HL) into the start address of TXFIFO. This length indicates that HL bytes in front of the data that the user wants to send will not be encrypted.

Step 2.

Load the frame into one of the four TXFIFOs that the user wants to send with encryption. The format is the same as Normal FIFO.

Step 3.

Load the nonce into LREG0x240 - 0x24C. About the nonce structure, please refer to Figure 77 of IEEE 802.15.4 - 2006.

Memory address	LSB	0x240 - 0x24C	MSB
Field size	1 byte	4 bytes	8 bytes
TX FIFO content	Security Level	Frame counter	Source MAC address

Step 4.

Fill in the corresponding key into the key table memory

Security Key	Address
Normal FIFO key	0x280 – 0x28F
GTS1 FIFO key	0x290 – 0x29F
GTS2/Beacon FIFO key	0x2A0 – 0x2AF

Step 5.

Fill in cipher mode

Normal FIFO cipher mode	SREG0x2C[2:0]
Beacon FIFO cipher mode	SREG0x2D[6:4]
GTS1 FIFO cipher mode	SREG0x37[2:0]
GTS2 FIFO cipher mode	SREG0x37[5:3]

Security mode value:

security mode	mode value
ENC	0x1
ENC_MIC 128	0x2
ENC_MIC 64	0x3
ENC_MIC 32	0x4
MIC 128	0x2
MIC 64	0x3
MIC 32	0x4

Step 6.

Trigger to encrypt the content in the FIFO and send it

Normal FIFO	SREG0x1B[1:0] = '11'
Beacon FIFO	SREG0x1A[1:0] = '11'
GTS1 FIFO	SREG0x1C[1:0] = '11'
GTS2 FIFO	SREG0x1D[1:0] = '11'

Step 7.

Wait for the FIFO to release the interrupt status as a plain text packet does.

Registers Associated with Transmit Packet with Security Encryption

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x1A	TXBTRIG	r	r	r	r	r	r	TXBCNSECEN	TXBCNTRIG	0000 0000
0x1B	TXNTRIG	r	r	r	PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG	0000 0000
0x1C	TXG1TRIG	TXG1IFETRY1	TXG1IFETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG	0000 0000
0x1D	TXG2TRIG	TXG2IFETRY1	TXG2IFETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG	0000 0000
0x2C	SECCR0	SECIGNORE	SECSTART	RXCIPHER2	RXCIPHER1	RXCIPHER0	TXNCIPHER2	TXNCIPHER1	TXNCIPHER0	0000 0000
0x2D	SECCR1	r	TXBCIPHER2	TXBCIPHER1	TXBCIPHER0	MACTMRFR	r	DISDEC	DISENC	0000 0000
0x37	SECCR2	UPDEC	UPENC	TXG2CIPHER2	TXG2CIPHER1	TXG2CIPHER0	TXG1CIPHER2	TXG1CIPHER1	TXG1CIPHER0	0000 0000
0x240	UPNONCE_0	UPNONCE[7:0]								0000 0000
0x241	UPNONCE_1	UPNONCE[15:8]								0000 0000
0x242	UPNONCE_2	UPNONCE[23:16]								0000 0000
0x243	UPNONCE_3	UPNONCE[31:24]								0000 0000
0x244	UPNONCE_4	UPNONCE[39:32]								0000 0000
0x245	UPNONCE_5	UPNONCE[47:40]								0000 0000
0x246	UPNONCE_6	UPNONCE[55:48]								0000 0000
0x247	UPNONCE_7	UPNONCE[63:56]								0000 0000
0x248	UPNONCE_8	UPNONCE[71:64]								0000 0000
0x249	UPNONCE_9	UPNONCE[79:72]								0000 0000
0x24A	UPNONCE_10	UPNONCE[81:80]								0000 0000
0x24B	UPNONCE_11	UPNONCE[95:88]								0000 0000
0x24C	UPNONCE_12	UPNONCE[89:96]								0000 0000

4.4.4. Transmit Packet in Normal FIFO with CCA/ED mode or combination of CS and ED modes

To send a packet in Normal FIFO with CCA/ED mode or combination of CS and ED modes, there are several steps to follow:

Step 1.

Fill in Normal FIFO with the packet to send. The format is as follows

TXFIFO Address 0x000			2+M+N
1 Byte	1 Bytes	M Bytes	N Bytes
Header length*1	Frame length*2	Header	Payload

*1: only lower 6 bits are valid.

*2: Value range is 1-125

Table 17: Normal FIFO format

Step 2.

Set an Ackreq in SREG0x1B[2] if an acknowledgement from the receiver is required. If the Ackreq is set, the UZ2400 automatically retransmits the packet if no acknowledgement is sent back. The UZ2400 will retransmit the packet till the number of the Max trial times specified by IEEE 802.15.4 is reached.

Step 3.

Set CCA to ED mode (SREG0x3A[7:6]=0b10) or combination of CS and ED modes (SREG0x3A[7:6]=0b11)

Step 4.

Set the trigger bit SREG0x1B[0] to send a packet. This bit will be automatically cleared. At this time, the TXMAC will perform CSMA-CA and send the packet at the right moment.

Step 5.

Wait for the interrupt status shown in SREG0x31[0].

Step 6.

Set CCA back to CS mode (SREG0x3A[7:6]=0b01)

Step 7.

Check SREG0x24[0] to see if transmission is successful. SREG0x24[0]=0 means transmission was successful and the ACK was received. The number of times of the retransmission can be read at SREG0x24[7:6]. SREG0x24[0]=1 means transmission failed and ACK was not received.

Registers Associated with Transmit Packet in Normal FIFO with CCA/ED mode or combination of CS and ED mode

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x1B	TXNTRIG	r	r	r	PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG	0000 0000
0x24	TXSR	TXRETRY1	TXRETRY 0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS	0000 0000
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000
0x3A	BBREG2	CCAMODE1	CCAMODE 0	CCATH3	CCATH2	CCATH1	CCATH0	r	r	0111 1111

4.5. Typical RX Operations

The UZ2400 RX PHY filters all incoming signals and tracks the synchronization symbols. When the preamble of an IEEE802.15.4 packet is found, the packet is demodulated and stored in the RXFIFO. At the same time, the RXMAC starts calculating the frame FCS byte by byte and checking after received a whole packet. The RXMAC filters the MAC header and skips those packets not being sent to own addresses. If the packet is acceptable and needs an acknowledgement, the RXMAC will inform the TXMAC to send an ACK packet automatically.

4.5.1. Receive Packet in RXFIFO

RXFIFO Address 0x300				0x300+m+n+3	0x300+m+n+4
1 Byte	M Byte	N Bytes	2 Byte	1 Byte	1 Byte
Frame length	MAC Header	MAC Payload	MAC FCS	LQI	RSSI

In the above table, 'Frame length' (in bytes) field includes the lengths of the header, the payload, and FCS (2 bytes), but it does not include LQI (1 byte) and RSSI (1 byte). When a packet passes the baseband filtering (preamble and delimiter), it goes into the RXMAC. The RXMAC performs several levels of the packet filtering.

Default mode is address-recognition mode, which can filter those packets not being sent to this device and/or others conforming to Section 7.5.6.2 of IEEE 802.15.4-2006 specifications. When a received packet passes the filters discussed above and has the correct FCS, an interrupt is issued at SREG0x31[3]. The MCU host can read the whole packet inside the RXFIFO. The RXFIFO is flushed when the length field of RXFIFO and the last byte of the frme are read, or when the host triggers a RX flush at SREG0x0D[0].

Registers Associated with Receive Packet in RXFIFO

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x0D	RXFLUSH	r	WAKEPOL	WAKEPAD	r	NOCSMATXN	r	r	RXFLUSH	0110 0000
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000

4.5.2. Receive Packet with Security Decryption

Configuring the UZ2400 to receive and decrypting a ciphered packet can be done by the following steps:

Step 1.

When a packet comes with the security enabled bit set in the frame control field of the packet header, a security interrupt, SREG0x31[4], is issued right after the complete packet header is received.

Step 2.

Check LREG0x21E for received header length. This header length of the received packet only includes frame control field, sequence number and address information. User can use the length to find out the RXFIFO start address of AXU security header.

Step 3.

Rewrite the LREG0x21E to tell UZ2400 that the real un-encrypted length of the received frame. The length will be used during the decryption process. It does not include the length of MIC code.

Step 4.

Check LREG0x212[1:0] for the source address mode of the received packet. If LREG0x212[1:0]='10' (short address), user should load the 64-bit long address of source device to LREG0x213 ~ LREG0x21A, LSB first. The 64-bit long address will be needed when the decryption is processed.

Step 5.

Load the nonce into LREG0x240 - 0x24C. About the nonce structure, please refer to Figure 77 of IEEE 802.15.4 - 2006. User can get the source MAC address from the received header of the packet, the self database or the address mapping table. The security level and frame counter can be fetched from the AUX security header field.

Memory address	*LSB*	*0x240 - 0x24C*	*MSB*
Field size	*1 byte*	*4 bytes*	*8 bytes*
TX FIFO content	Security Level	Frame counter	Source MAC address

Step 6.

According to the content of the received AUX security header, the host should perform the key searching and fill in the key FIFO of RX with the suitable security key.

Security Key	Address
RXFIFO key	0x2B0 – 0x2BF

Step 7.

Besides setting the RXFIFO key, the MCU host should also perform the security mode decision and set the corresponding cipher mode in SREG0x2C[5:3].

After both the key and the security mode are set, the security engine should be configured and enabled by setting SREG0x2C[6]=1. If there is no suitable key for the received packet, user can ignore the decryption process this time by setting the short register SREG0x2C[7]=1.

Step 8.

After the packet is successfully decrypted or the decryption is ignored, an RX interrupt is issued to notify that the whole processes of receiving and decryption has been done. User can check the error status from SREG0x30[2]. If SREG0x30[2]='0', the decrypted data is available in RXFIFO. If SREG0x30[2]='1', it means decryption failed and user must perform RXFIFO flush by setting SREG0x0D[0].

Registers Associated with Receive Packet with Security Decryption

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x0D	RXFLUSH	r	WAKEPOL	WAKEPAD	r	NOCSMATXN	r	r	RXFLUSH	0110 0000
0x2C	SECCR0	SECIGNORE	SECSTART	RXCIPHER2	RXCIPHER1	RXCIPHER0	TXNCIPHER2	TXNCIPHER1	TXNCIPHER0	0000 0000
0x30	RXSR	RXFFFULL	WRFF1	UPSECERR	RXFFOVFL	RXCRCERR	SECDECERR	r	r	0000 0000
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000
0x212	SADRCTRL	r	r	r	r	r	r	SADRMODE1	SADRMODE0	0000 0000
0x213	SRCADR_0	SRCADR7	SRCADR6	SRCADR5	SRCADR4	SRCADR3	SRCADR2	SRCADR1	SRCADR0	0000 0000
0x214	SRCADR_1	SRCADR15	SRCADR14	SRCADR13	SRCADR12	SRCADR11	SRCADR10	SRCADR9	SRCADR8	0000 0000
0x215	SRCADR_2	SRCADR23	SRCADR22	SRCADR21	SRCADR20	SRCADR19	SRCADR18	SRCADR17	SRCADR16	0000 0000
0x216	SRCADR_3	SRCADR31	SRCADR30	SRCADR29	SRCADR28	SRCADR27	SRCADR26	SRCADR25	SRCADR24	0000 0000
0x217	SRCADR_4	SRCADR39	SRCADR38	SRCADR37	SRCADR36	SRCADR35	SRCADR34	SRCADR33	SRCADR32	0000 0000
0x218	SRCADR_5	SRCADR47	SRCADR46	SRCADR45	SRCADR44	SRCADR43	SRCADR42	SRCADR41	SRCADR40	0000 0000
0x219	SRCADR_6	SRCADR55	SRCADR54	SRCADR53	SRCADR52	SRCADR51	SRCADR50	SRCADR49	SRCADR48	0000 0000
0x21A	SRCADR_7	SRCADR63	SRCADR62	SRCADR61	SRCADR60	SRCADR59	SRCADR58	SRCADR57	SRCADR56	0000 0000
0x21E	HLEN	r	r	HLEN5	HLEN4	HLEN3	HLEN2	HLEN1	HLEN0	0000 0000
0x240	UPNONCE_0	UPNONCE[7:0]								0000 0000
0x241	UPNONCE_1	UPNONCE[15:8]								0000 0000
0x242	UPNONCE_2	UPNONCE[23:16]								0000 0000
0x243	UPNONCE_3	UPNONCE[31:24]								0000 0000
0x244	UPNONCE_4	UPNONCE[39:32]								0000 0000
0x245	UPNONCE_5	UPNONCE[47:40]								0000 0000
0x246	UPNONCE_6	UPNONCE[55:48]								0000 0000
0x247	UPNONCE_7	UPNONCE[63:56]								0000 0000

0x248	UPNONCE_8	UPNONCE[71:64]	0000 0000
0x249	UPNONCE_9	UPNONCE[79:72]	0000 0000
0x24A	UPNONCE_10	UPNONCE[81:80]	0000 0000
0x24B	UPNONCE_11	UPNONCE[95:88]	0000 0000
0x24C	UPNONCE_12	UPNONCE[89:96]	0000 0000

4.6. Beacon Mode Operations

4.6.1. Beacon Mode Setting

Beacon Mode for Coordinator

Step 1.

Avoid beacon transmitted by setting SREG0x10 to '0xFF'.

Step 2.

Configure the UZ2400 to slotted mode by setting SREG0x11[5] to '1'.

Step 3.

Configure the UZ2400 as the PAN Coordinator by setting SREG0x00[3] to '1'.

Step 4.

Prepare the beacon frame content and fill it in the TX Beacon FIFO.

Beacon FIFO Address 0x080			82+M+N
1 Byte	1 Bytes	M Bytes	N Bytes
Header length*1	Frame length*2	Header	Payload

*1: only lower 6 bits are valid.

*2: Value range is 1-125

Table 18: Beacon FIFO format

Step 5.

Set the beacon interrupt mask by setting SREG0x25[7] to '1'.

Step 6.

Configure the interval to start beacon after beacon is triggered by setting SREG0x22[5:0] to '0x03'.

Step 7.

Select the sleep clock source. If the internal sleep clock is used, set LREG0x275[4] to '1'. Or if an external crystal is used, set LREG0x275[4] to '0'.

Step 8.

Configure system clock (32 MHz) recovery time WAKECNT = {SREG0x36[4:3], SREG0x35[6:0]}. If the internal sleep clock is used, user needs to calibrate the sleep clock frequency. Refer to Section 4.3.2. Clock Recovery Time for detail procedure.

Step 9.

Configure the timer WAKETIME {LREG0x223, LREG0x222} to wake system clock up. WAKETIME should be larger than WAKECNT.

Step 10.

Calculate the MainCNT and RemainCNT according to BO and SO.

aBaseSuperframeDuration = 60 symbols x 16 us x 16 slots = 15360 us
Beacon _interval = aBaseSuperframeDuration * (2^BO)

MainCNT = (Beacon_interval – (4 * Psleepclock)) / Psleepclock
RemainCNT = (Beacon_interval – MainCNT * Psleepclock) / 62.5 ns

Main Counter is a 26-bit compound register.
LREG0x229 [1:0] = main counter [25:24]
LREG0x228 [7:0] = main counter [23:16]
LREG0x227 [7:0] = main counter [15:8]
LREG0x226 [7:0] = main counter [7:0]

Remain Counter is a 16-bit compound register.
LREG0x225 [7:0] = remain counter [15:8]
LREG0x224 [7:0] = remain counter [7:0]

Step 11

Configure the BO and SO values by setting SREG0x10. After configuring BO and SO, the beacon frame will be sent immediately.

Beacon Mode for Device

Step 1.

Avoid beacon transmitted by setting SREG0x10 to '0xFF'.

Step 2.

Configure the UZ2400 to slotted mode by setting SREG0x11[5] to '1'.

Step 3.

Set SREG0x23 to the value '0x15' for more accurate time alignment.

Step 4.

Configure the interval to start beacon after beacon is triggered by setting SREG0x22 '0x03'

Step 5.

Program the coordinator address for time alignment at LREG0x230 ~ LREG0x239.
Note that a device will align a beacon frame only when the source address of the beacon frame is identical to LREG0x230~LREG0x237 (64-bit extended address mode) or LREG0x238~LREG0x239 (16-bit short address mode)

Step 6.

Select the sleep clock source. If the internal sleep clock is used, set LREG0x275[4] to '1'. Or if an external crystal is used, set LREG0x275[4] to '0'.

Step 7.

Configure system clock (32 MHz) recovery time WAKECNT = {SREG0x36[4:3], SREG0x35[6:0]}. If the internal sleep clock is used, user needs to calibrate the sleep clock frequency. Refer to Section 4.3.2. Clock Recovery Time for detail procedure.

Step 8.

Configure the timer WAKETIME {LREG0x223, LREG0x222} to wake system clock up. WAKETIME should be larger than WAKECNT.

Step 9.

Calculate the MainCNT / RemainCNT according to BO and SO.

aBaseSuperframeDuration = 60 symbols x 16 us x 16 slots = 15360 us
Inactive_interval = aBaseSuperframeDuration * (2^BO - 2^SO)

MainCNT = (Inactive_interval – (4 * Psleepclock)) / Psleepclock
RemainCNT = (Inactive_interval – MainCNT * Psleepclock) / 62.5 ns

Main Counter is a 26-bit compound register.
LREG0x229 [1:0] = main counter [25:24]
LREG0x228 [7:0] = main counter [23:16]
LREG0x227 [7:0] = main counter [15:8]
LREG0x226 [7:0] = main counter [7:0]

Remain Counter is a 16-bit compound register.
LREG0x225 [7:0] = remain counter [15:8]
LREG0x224 [7:0] = remain counter [7:0]

Step 10.

Configure the BO and SO values by setting SREG0x10. After configuring BO and SO, the beacon frame will be sent immediately.

Registers Associated with Beacon Mode Setting

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x00	RXMCR	r	r	NOACKRSP	r	PANCOORD	COORD	r	r	0000 0000
0x10	ORDER	BO3	BO2	BO1	BO0	SO3	SO2	SO1	SO0	1111 1111
0x11	TXMCR	NOCSMAG	r	SLOTTED	MACMINBE1	MACMINBE0	CSMABF2	CSMABF1	CSMABF0	0001 1100
0x22	WAKECTL	IMMWAKE	REGWAKE	INTL5	INTL4	INTL3	INTL2	INTL1	INTL0	0000 0000
0x23	ALIGNOFF	AOFFSET7	AOFFSET6	AOFFSET5	AOFFSET4	AOFFSET3	AOFFSET2	AOFFSET1	AOFFSET0	0000 0000
0x25	TXBCNMSK	TXBCNMSK	r	r	r	r	r	r	r	0011 0000
0x35	SLPACK	SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0	0000 0000
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE	0000 0000
0x209	SLPCAL_0	SLPCAL7	SLPCAL6	SLPCAL5	SLPCAL4	SLPCAL3	SLPCAL2	SLPCAL1	SLPCAL0	0000 0000
0x20A	SLPCAL_1	SLPCAL15	SLPCAL14	SLPCAL13	SLPCAL12	SLPCAL11	SLPCAL10	SLPCAL9	SLPCAL8	0000 0000
0x20B	SLPCAL_2	SLPCALRDY	r	r	SLPCALEN	SLPCAL19	SLPCAL18	SLPCAL17	SLPCAL16	0000 0000
0x220	SLPCTRL	r	r	r	SCLKDIV4	SCLKDIV3	SCLKDIV2	SCLKDIV1	SCLKDIV0	0000 0000
0x222	WAKETIMEL	WAKETIME7	WAKETIME6	WAKETIME5	WAKETIME4	WAKETIME3	WAKETIME2	WAKETIME1	WAKETIME0	0000 1010
0x223	WAKETIMEH	r	r	r	r	r	WAKETIME10	WAKETIME9	WAKETIME8	0000 0000
0x224	REMCNTL	REMCNT7	REMCNT6	REMCNT5	REMCNT4	REMCNT3	REMCNT2	REMCNT1	REMCNT0	0000 0000
0x225	REMCNTH	REMCNT15	REMCNT14	REMCNT13	REMCNT12	REMCNT11	REMCNT10	REMCNT9	REMCNT8	0000 0000
0x226	MAINCNT_0	MAINCNT7	MAINCNT6	MAINCNT5	MAINCNT4	MAINCNT3	MAINCNT2	MAINCNT1	MAINCNT0	0000 0000
0x227	MAINCNT_1	MAINCNT15	MAINCNT14	MAINCNT13	MAINCNT12	MAINCNT11	MAINCNT10	MAINCNT9	MAINCNT8	0000 0000
0x228	MAINCNT_2	MAINCNT23	MAINCNT22	MAINCNT21	MAINCNT20	MAINCNT19	MAINCNT18	MAINCNT17	MAINCNT16	0000 0000
0x229	MAINCNT_3	STARTCNT	r	r	r	r	r	MAINCNT25	MAINCNT24	0000 0000
0x230	ASSOEADR_0	ASSOEADR[7:0]								0000 0000
0x231	ASSOEADR_1	ASSOEADR[15:8]								0000 0000
0x232	ASSOEADR_2	ASSOEADR[23:16]								0000 0000
0x233	ASSOEADR_3	ASSOEADR[31:24]								0000 0000
0x234	ASSOEADR_4	ASSOEADR[39:32]								0000 0000
0x235	ASSOEADR_5	ASSOEADR[47:40]								0000 0000
0x236	ASSOEADR_6	ASSOEADR[55:48]								0000 0000
0x237	ASSOEADR_7	ASSOEADR[63:56]								0000 0000
0x238	ASSOSADRL	ASSOSADR[7:0]								0000 0000
0x239	ASSOSADRH	ASSOSADR[15:8]								0000 0000
0x275	RFCTRL75	r	r	r	SCLKSEL	SCLKOPT3	SCLKOPT2	SCLKOPT1	SCLKOPT0	0001 0101

4.6.2. Beacon Mode GTS Setting

GTS for Coordinator

Step 1.

Configure the CAP and CFP. Program the end slot of the CAP and each GTS.

- SREG0x13 for the CAP and 1st GTS.
- SREG0x1E for the 2nd GTS and 3rd GTS.
- SREG0x1F for the 4th GTS and 5th GTS.
- SREG0x20[3:0] for the 6th GTS.

Note that there is no end slot configuration for the 7th GTS. This is because if the 7th GTS is present, then the value of its end slot must be '0x0F', the last slot of the active period.

Step 2.
Enable GTS FIFO clock by setting SREG0x26[3] to '1'.

Step 3.
Fill in the GTS FIFO with a packet to send. The format is the same as Normal FIFO.

Step 4.
Set an Ackreq in {SREG0x1C[2], SREG0x1D[2]} if an acknowledgement from the receiver is required. If the Ackreq is set, the UZ2400 automatically retransmits the packet if there is no acknowledgement sent back. The UZ2400 will retransmit the packet till the number of the Max trial times specified by IEEE 802.15.4 is reached or when the CFP is ended.

Step 5.
Set the corresponding GTS slot number in {SREG0x1C[5:3], SREG0x1D[5:3]} to decide when to send this packet in FIFO.

Step 6.
Set the retransmission time at SREG0x1C[7:6] and SREG0x1D[7:6] for GTS1 and GTS2 FIFO respectively.

Step 7.
Set the trigger bit {SREG0x1C[0], SREG0x1D[0]} to send the packet. This bit will be automatically cleared. At this time, the TXMAC will wait until the corresponding GTS slot sends the packet at that moment.

Step 8.
Wait for the interrupt status shown in SREG0x31[1] for GTS1 FIFO and SREG0x31[2] for GTS2 FIFO.

Step 9.
Check SREG0x24[1] or SREG0x24[2] to see if transmission is successful. SREG0x24[1]=0 or SREG0x24[2]=0 mean transmission successful and the ACK was received. The number of times of the re-transmission can be read at SREG0x1C[7:6] or SREG0x1D[7:6]. SREG0x24[1]=1 or SREG0x24[2]=1 mean transmission failed and ACK was not received.

GTS for Devices
Step 1.
Parse the received beacon frame to obtain the GTS allocation information. Then program the end slot of the CAP and each GTS the same way as step 1 for the Coordinator.

Step 2.
Enable GTS FIFO clock by setting SREG0x26[3] to '1'.

Step 3.
Fill in the GTS FIFO with a packet to send. The format is the same as Normal FIFO.

Step 4.

Set an Ackreq in {SREG0x1C[2], SREG0x1D[2]} if an acknowledgement from the receiver is required. If the Ackreq is set, the UZ2400 automatically retransmits the packet if there is no acknowledgement received. The UZ2400 will retransmit till the number of the Max trial times specified by IEEE 802.15.4 is reached or when the CFP is ended.

Step 5.

Set the corresponding GTS slot number in {SREG0x1C[5:3], SREG0x1D[5:3]} to decide when to send this packet in FIFO.

Step 6.

Set the retransmission time at SREG0x1C[7:6] and SREG0x1D[7:6] for GTS1 and GTS2 FIFO respectively.

Step 7.

Set the trigger bit {SREG0x1C[0], SREG0x1D[0]} to send the packet. This bit will be automatically cleared. At this time, the TXMAC will wait until the corresponding GTS slot sends the packet at that moment.

Step 8.

Wait for the interrupt status shown in SREG0x31[1] for GTS1 FIFO and SREG0x31[2] for GTS2 FIFO.

Step 9.

Check SREG0x24[1] or SREG0x24[2] to see if transmission is successful. SREG0x24[1]=0 or SREG0x24[2]=0 mean transmission successful and the ACK was received. The number of times of the re-transmission can be read at SREG0x1C[7:6] or SREG0x1D[7:6]. SREG0x24[1]=1 or SREG0x24[2]=1 mean transmission failed and ACK was not received.

Registers Associated with Beacon Mode GTS Setting

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x13	ESLOTG1C	GTS1-3	GTS1-2	GTS1-1	GTS1-0	CAP3	CAP2	CAP1	CAP0	0000 0000
0x1C	TXG1TRIG	TXG1IFETRY1	TXG1IFETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG	0000 0000
0x1D	TXG2TRIG	TXG2IFETRY1	TXG2IFETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG	0000 0000
0x1E	ESLOTG23	GTS3-3	GTS3-2	GTS3-1	GTS3-0	GTS2-3	GTS2-2	GTS2-1	GTS2-0	0000 0000
0x1F	ESLOTG45	GTS5-3	GTS5-2	GTS5-1	GTS5-0	GTS4-3	GTS4-2	GTS4-1	GTS4-0	0000 0000
0x20	ESLOTG6	r	r	r	r	GTS6-3	GTS6-2	GTS6-1	GTS6-0	0000 0000
0x24	TXSR	TXRETRY1	TXRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS	0000 0000
0x26	GATECLK	r	r	SPISYNC	ENRXM	ENGTS	ENTXM	r	r	0000 0000
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000

4.7. Power Saving Operations

To balance between current consumption and wake-up time, there are five power saving modes in total defined in UZ2400, i.e. Idle, Halt, Standby, Deep-Sleep and Power-Down mode.

4.7.1. Wake-up Operations

After entering into power saving mode, UZ2400 need to be waked-up to Active mode for data transmission or reception. Three methods to wake UZ2400 up and back to active mode are available for different modes, i.e. by WAKE pin, by register trigger and timed wake-up. One and only one method should be used for wake-up operation.

WAKE Pin Wake-up

Wake-up on WAKE pin can be used for Standby, Halt, Deep-Sleep and Power-Down modes.

Before entering into these power saving modes, the following steps shall be executed.
1. Enable the WAKE pin by setting SREG0x0D[5]=0:
2. Set SREG0x0D[6]=0 for active low polarity, or SREG0x0D[6]=1 for active high polarity of WAKE signal

To execute the following steps, to wake UZ2400 up from Standby, Halt and Deep-Sleep modes.
1. Trigger WAKE pin with pre-defined polarity.
2. Wait UZ2400 issues wake-up interrupt. SREG0x31[6]
3. If SPISYNC function is needed , turn it on. SREG0x26[5]=1.
4. If DC-DC enabled is needed, turn it on. LREG0x250[4]=1.

To execute the following steps, to wake UZ2400 up from Power-Down modes.
1. Trigger WAKE pin with pre-defined polarity.
2. Initialize UZ2400 by the settings described in Section 4.3.1

Register Trigger

Wake-up by the register triggering can be used in Halt and Standby modes. One can wake UZ2400 up from Halt mode and Standby mode by executing the following steps.
1. Set SREG0x22[7:6]='11'. SREG0x22[6] will be automatically cleared to the value '0'.
2. Wait UZ2400 issue wake-up interrupt. SREG0x31[6]
3. If SPISYNC function is needed , turn it on. SREG0x26[5]=1.
4. If DC-DC enabled is needed, turn it on. LREG0x250[4]=1.
5. Set SREG0x22[7]='0'.

Timed Wake-up

Wake-up by the timer can be used in Halt and Standby modes. Before entering into these power saving modes, the counters for power saving mode should be set properly. Please refer to Section 3.4.6 and 4.3.2 for detail information.

To execute the following steps, to wake UZ2400 up from Standby, Halt modes.
1. Wait UZ2400 issues wake-up interrupt. SREG0x31[6]

2. If SPISYNC function is needed , turn it on. SREG0x26[5]=1.
3. If DC-DC enabled is needed, turn it on. LREG0x250[4]=1.

Registers Associated with Wake-up Operations

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x0D	RXFLUSH	r	WAKEPOL	WAKEPAD	r	NOCSMATXN	r	r	RXFLUSH	0110 0000
0x22	WAKECTL	IMMWAKE	REGWAKE	INTL5	INTL4	INTL3	INTL2	INTL1	INTL0	0000 0000
0x26	GATECLK	r	r	SPISYNC	ENRXM	ENGTS	ENTXM	r	r	0000 0000
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000
0x250	RFCTRL50	r	r	r	DCPOC	DCOPC3	DCOPC2	DCOPC1	DCOPC0	0000 0000

4.7.2. Power Saving Operations

It is only allowed to switch between power saving mode and active mode, whereas it is not able to switch between different power saving modes. The settings to enter into the power saving mode are only effective in active mode.

IDLE Mode:

RF circuit shutdown while the MAC/BB, system and sleep clocks remain active. To enter into Idle Mode just simply by setting SREG0x36[2] to '1' to hold RF state machine in Reset. To release the hold status by set SREG0x36[2] back to '0'.

HALT Mode:

RF/MAC/BB shutdown while the system clock, clock output and the sleep clock remain active. Halt mode is the only power saving mode which supports clock output function.

Be sure the following settings are set correctly before entering in Halt mode.

- Keep the same output clock frequency used in active mode or select another one by LREG0x207[7:5].
- Set LREG0x277[3:2] to '01' for enable sleep voltage controlled by LREG0x277[1:0]
- Enable Halt mode control by setting LREG0x255[5]='1'
- The setting for WAKE pin and Timed wake-up should be included. Refer to Section 4.7.1 for details.
- If DC-DC is used, bypass it by setting LREG0x250[4] to '0'.
- Set SREG0x26[5] to '0' to disable SPISYNC

If user wants to wake UZ2400 up by WAKE pin or register trigger, set SREG0x35[7]=1 to place UZ2400 to Halt mode. Otherwise, set LREG0x229[7]=1 for timed wake up.

STANDBY Mode:

RF/MAC/BB shutdown while the sleep clock remains active.

Be sure the following settings are set correctly before entering in Standby mode.

- Set LREG0x277[5:4] to '00' to select for Standby mode
- Set LREG0x277[3:2] to '10' for enable sleep voltage automatically controlled by internal circuit
- The setting for WAKE pin and Timed wake-up should be included. Refer to Section 4.7.1 for details.
- If DC-DC is used, bypass it by setting LREG0x250[4] to '0'.

- Set SREG0x26[5] to '0' to disable SPISYNC

If user wants to wake UZ2400 up by WAKE pin or register trigger, set SREG0x35[7]=1 to place UZ2400 to Standby mode. Otherwise, set LREG0x229[7]=1 for timed wake up.

DEEP SLEEP Mode:

All power is shutdown except the power to the digital circuits. Register and FIFO data are retained. Only external wake-up signal can wake up the UZ2400.

Be sure the following settings are set correctly before entering in Deep-Sleep mode.

- Set LREG0x277[5:4] to '01' to select for Deep Sleep mode
- Set LREG0x277[3:2] to '10' for enable sleep voltage automatically controlled by internal circuit
- The setting for WAKE pin wake-up should be included. Refer to Section 4.7.1 for details.
- If DC-DC is used, bypass it by setting LREG0x250[4] to '0'.
- Set SREG0x26[5] to '0' to disable SPISYNC

UZ2400 can only be waked up by WAKE pin. Set SREG0x35[7]=1 to place UZ2400 to Deep-Sleep mode.

POWER DOWN Mode:

In Power-Down mode, all power is shutdown. Register and FIFO data are not retained. After waked up by WAKE pin, the UZ2400 will not issue wake-up alert interrupt. The initialization described in Section 4.3.1 should be configured after UZ2400 back to active mode. Only external wake-up signal can wake up the UZ2400.

Be sure the following settings are set correctly before entering in Power-Down mode.

- Set LREG0x277[5:4] to '11' to select for Power Down mode
- Set LREG0x277[3:2] to '10' for enable sleep voltage automatically controlled by internal circuit
- Set LREG0x253[6:5] to '11' to connect the FIFO power and digital circuit power to ground
- The setting for WAKE pin wake-up should be included. Refer to Section 4.7.1 for details.
- If DC-DC is used, bypass it by setting LREG0x250[4] to '0'.
- Set SREG0x26[5] to '0' to disable SPISYNC

UZ2400 can only be waked up by WAKE pin. Set SREG0x35[7]=1 to place UZ2400 to Power-Down mode.

Registers Associated with Power Saving Operations

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x26	GATECLK	r	r	SPISYNC	ENRXM	ENGTS	ENTXM	r	r	0000 0000
0x35	SLPACK	SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0	0000 0000
0x36	RFCTL	r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE	0000 0000
0x207	RFCTRL7	OUTCLK2	OUTCLK1	OUTCLK0	RXFC2	TXFS1	TXFS0	r	r	0000 0000
0x229	MAINCNT_3	STARTCNT	r	r	r	r	r	MAINCNT25	MAINCNT24	0000 0000
0x250	RFCTRL50	r	r	r	DCPOC	DCOPC3	DCOPC2	DCOPC1	DCOPC0	0000 0000
0x253	RFCTRL53	r	FIFOPS	DIGITALPS	r	PA1CFEN	PA1CTRLF-2	PA1CTRLF-1	PA1CTRLF-0	0000 0000
0x255	RFCTRL55	r	r	HALTCTRL	r	r	r	r	r	0000 0000
0x277	RFCTRL77	r	r	SLPSEL1	SLPSEL0	SLPVCTRL	SLPVCTRL	SLPVSEL1	SLPVSEL0	0000 1000

4.8. Battery Monitor Operations

Step 1.
Set the battery monitor threshold value at LREG0x205[7:4].

Step 2.
Enable the battery monitor by setting the LREG0x206[3] to the value '1'.

Step 3.
Read the battery-low indicator at SREG0x34[5]. If this bit is set, it means that the supply voltage is lower than the threshold.

Registers Associated with Battery Monitor Operations

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x34	SPIRXF	r	r	BATIND	r	r	r	RDFF1	RXFIFO2	0000 0000
0x205	RFCTRL5	BATTH3	BATTH2	BATTH1	BATTH0	r	r	r	r	0000 0000
0x206	RFCTRL6	TXFBW1	TXFBW0	32MXCO1	32MCCO0	BATEN	r	r	r	1111 0000

4.9. Upper-Layer-Cipher Operations

4.9.1. Upper-Layer-Cipher Encryption

Here are the instructions for using TXNFIFO, TX Normal FIFO, to perform the Upper-Layer-cipher encryption:

Step 1.
Load data into the TXNFIFO with the following format:

Memory address	*0x000*	*0x001*	*0x002~(HL+1)*	*(HL+2)~(PL+HL+1)*
Field size	*1 (byte)*	*1 (byte)*	*HL (bytes)*	*PL (bytes)*
TX FIFO content	Header Length (HL)	Frame Length (FL)	Header	Payload

Frame length (FL)= Header length (HL) + payload length (PL)

Note that each cipher mode has different maximum frame length allowed as given in the following:

Upper cipher mode	Maximum input frame length for encryption
ENC	125 bytes
ENC-MIC-128 / MIC-128	109 bytes
ENC-MIC-64 / MIC-64	117 bytes
ENC-MIC-32 / MIC-32	121 bytes

Table 19: Maximum frame length for upper cipher encryption

Step 2.

Load CCM NONCE (13 bytes) into LREG0x240 - LREG0x24C. For detailed information, please refer to 7.6.3.2 CCM* Nonce of IEEE 802.15.4 - 2006.

Step 3.

Write the security key at address 0x280~ 0x28F as shown below.

Address	Description
0x280 ~ 0x28F	TX Normal FIFO key

Step 4.

Set cipher mode of the TXNFIFO at SREG0x2C[2:0].

security mode	mode value
ENC	0x1
ENC_MIC 128	0x2
ENC_MIC 64	0x3
ENC_MIC 32	0x4
MIC 128	0x2
MIC 64	0x3
MIC 32	0x4

Step 5.

Enable Upper-Layer-Cipher encryption by setting SREG0x37[6]='1'.

Step 6.

Trigger encryption by setting SREG0x1B[1:0]='11'.

Step 7.

Wait for the TxN interrupt, or check if SREG0x31[0]='1'.

Step 8.

Check SREG0x24[0]. If SREG0x24[0]=0, it means the encryption process is done.

Step 9

After ENC-MIC or MIC encryption, the AES integrity code (4, 8, or 16 bytes) shall be appended to frame payload and the frame length is updated automatically. The TX FIFO content before and after the encryption for the selected mode is shown in the following Figure.

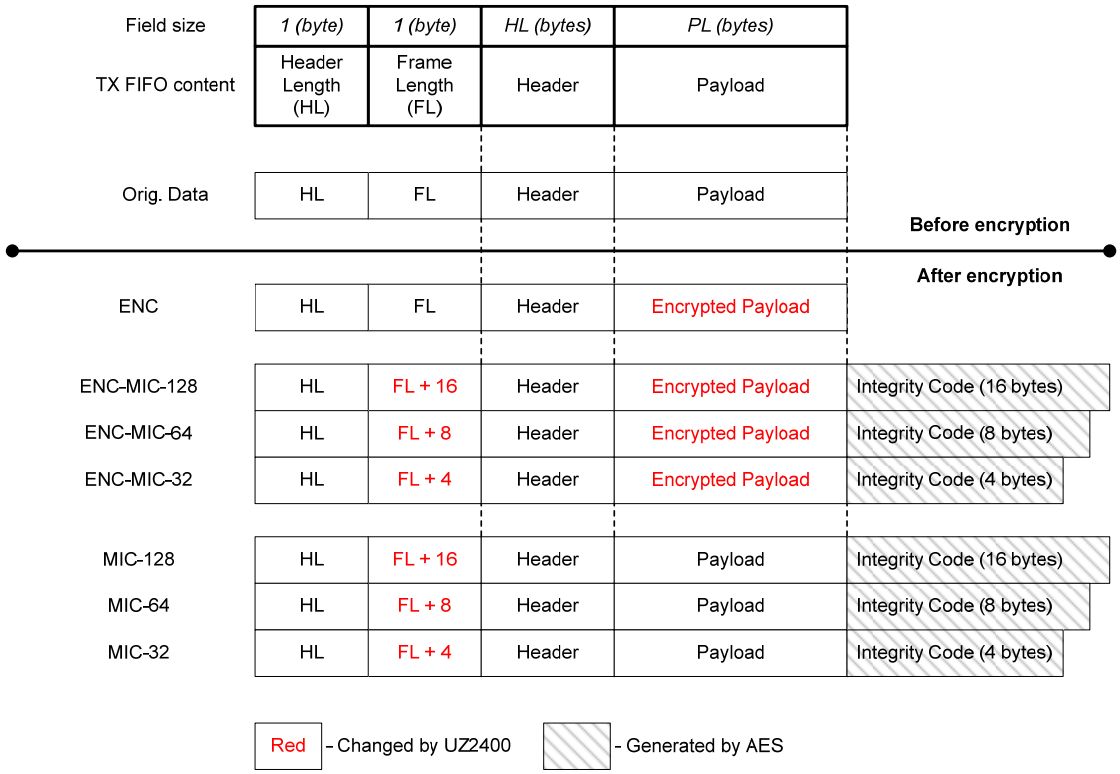


Figure 28: Upper-Layer-Cipher encryption

Registers Associated with Upper Cipher Encryption

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x1B	TXNTRIG	r	r	r	PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG	0000 0000
0x24	TXSR	TXRETRY1	TXRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS	0000 0000
0x2C	SECCR0	SECIGNORE	SECSTART	RXCIPHER2	RXCIPHER1	RXCIPHER0	TXNCIPHER2	TXNCIPHER1	TXNCIPHER0	0000 0000
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000
0x37	SECCR2	UPDEC	UPENC	TXG2CIPHER2	TXG2CIPHER1	TXG2CIPHER0	TXG1CIPHER2	TXG1CIPHER1	TXG1CIPHER0	0000 0000
0x240	UPNONCE_0	UPNONCE[7:0]								0000 0000
0x241	UPNONCE_1	UPNONCE[15:8]								0000 0000
0x242	UPNONCE_2	UPNONCE[23:16]								0000 0000
0x243	UPNONCE_3	UPNONCE[31:24]								0000 0000
0x244	UPNONCE_4	UPNONCE[39:32]								0000 0000
0x245	UPNONCE_5	UPNONCE[47:40]								0000 0000
0x246	UPNONCE_6	UPNONCE[55:48]								0000 0000
0x247	UPNONCE_7	UPNONCE[63:56]								0000 0000
0x248	UPNONCE_8	UPNONCE[71:64]								0000 0000
0x249	UPNONCE_9	UPNONCE[79:72]								0000 0000
0x24A	UPNONCE_10	UPNONCE[81:80]								0000 0000
0x24B	UPNONCE_11	UPNONCE[95:88]								0000 0000
0x24C	UPNONCE_12	UPNONCE[89:96]								0000 0000

4.9.2. Upper-Layer-Cipher Decryption

Here are the instructions for using TXNFIFO, TX Normal FIFO, to perform the Upper-Layer-cipher decryption:

Step 1.

Load the data to be decrypted into the TXNFIFO with the following format:

Memory address	*0x000*	*0x001*	*0x002~(HL+1)*	*(HL+2)~(PL+HL+1)*
Field size	*1 (byte)*	*1 (byte)*	*HL (bytes)*	*PL (bytes)*
TX FIFO content	Header Length (HL)	Frame Length (FL)	Header	Payload (with integrity code)

For ENC, frame length (FL) = header length (HL) + payload length (PL)
For ENC-MIC or MIC, the Frame length must be increased by 2 as shown below:
frame length (FL) = header length (HL) + payload length (PL) + 2

Step 2.

Write NONCE (13 bytes) at LREG0x240~ LREG 0x24C.

Step 3.

Write the security key at address 0x280~ 0x28F as shown below.

Address	Description
0x280 ~ 0x28F	TX Normal FIFO key

Step 4.

Set cipher mode of the TXNFIFO at SREG0x2C[2:0].

security mode	mode value
ENC	0x1
ENC_MIC 128	0x2
ENC_MIC 64	0x3
ENC_MIC 32	0x4
MIC 128	0x2
MIC 64	0x3
MIC 32	0x4

Step 5.

Enable Upper-Layer-Cipher decryption by setSREG0x37[7]='1'.

Step 6.

Trigger decryption by setting SREG0x1B[1:0]=11.

Step 7.

Wait for TxN interrupt, or check ISRSTS (SREG0x31[0]='1').

Step 8.

Check SREG0x24[0]. If SREG0x24[0]=0, it means the decryption process is done.

Step 9.

Check SREG0x30[5] for the MIC check error. If SREG0x30[5]='0', no error occurred.

Step 10.

The TX FIFO content before and after the decryption for the selected mode is shown in the following figure.

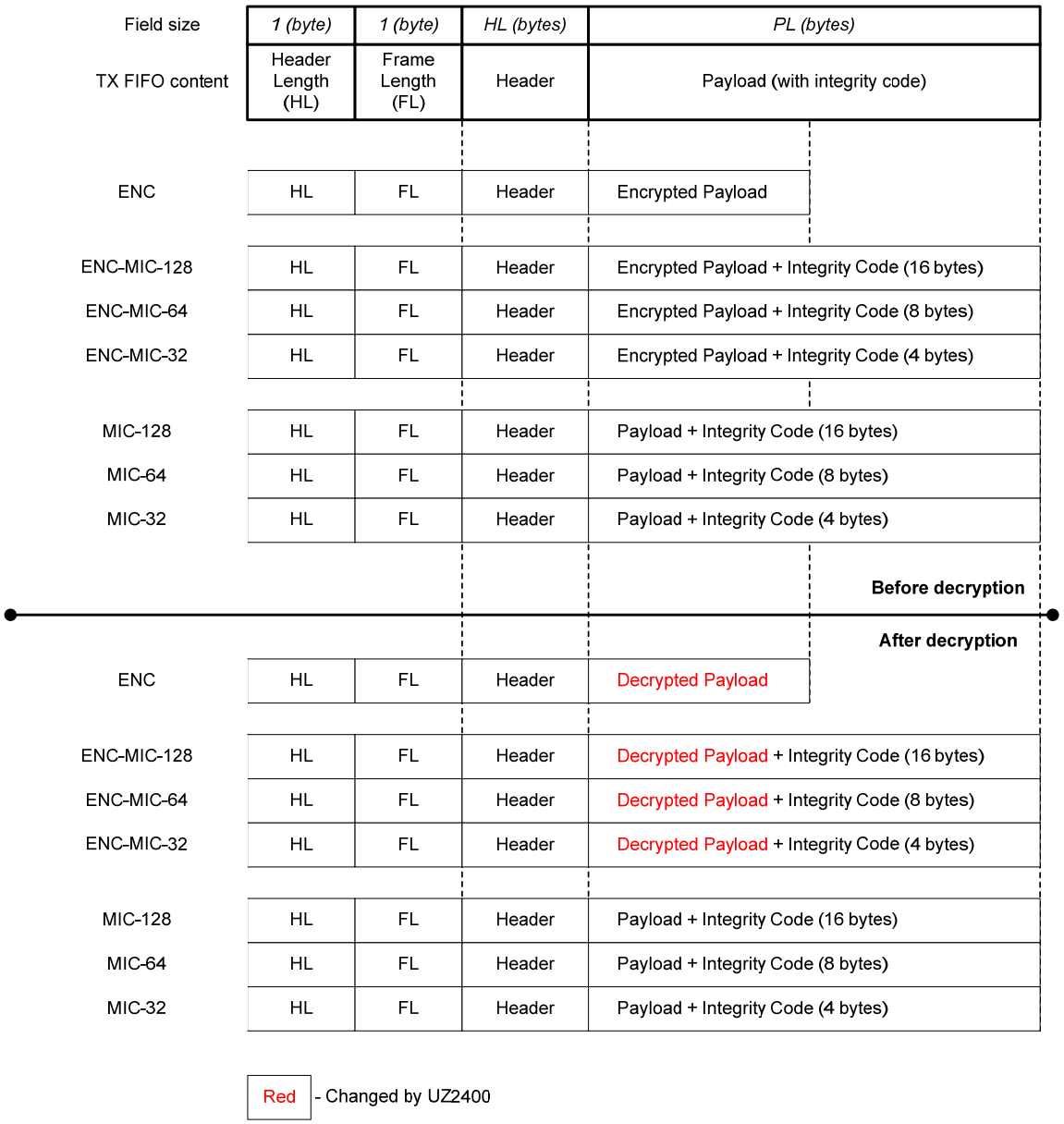


Figure 29: Upper-Layer-Cipher decryption

Step 11.

For the ENC-MIC and MIC modes, the frame length shown in TXFIFO will still include the integrity code length. Therefore it is recommended that the user use the following table to calculate the actual post-decryption header and payload lengths.

Upper cipher mode	Header length	Payload length without integrity code
ENC	HL	FL - HL
ENC-MIC-128 / MIC-128	HL	FL - HL - 16 - 2
ENC-MIC-64 / MIC-64	HL	FL - HL - 8 - 2
ENC-MIC-32 / MIC-32	HL	FL - HL - 4 - 2

Table 20: Post-decryption header and payload length

Step 12.

Based on the calculated head and payload lengths of Step 11, the decrypted data available in the TXNFIFO can be read by the host microcontroller

Registers Associated with Upper Cipher Encryption

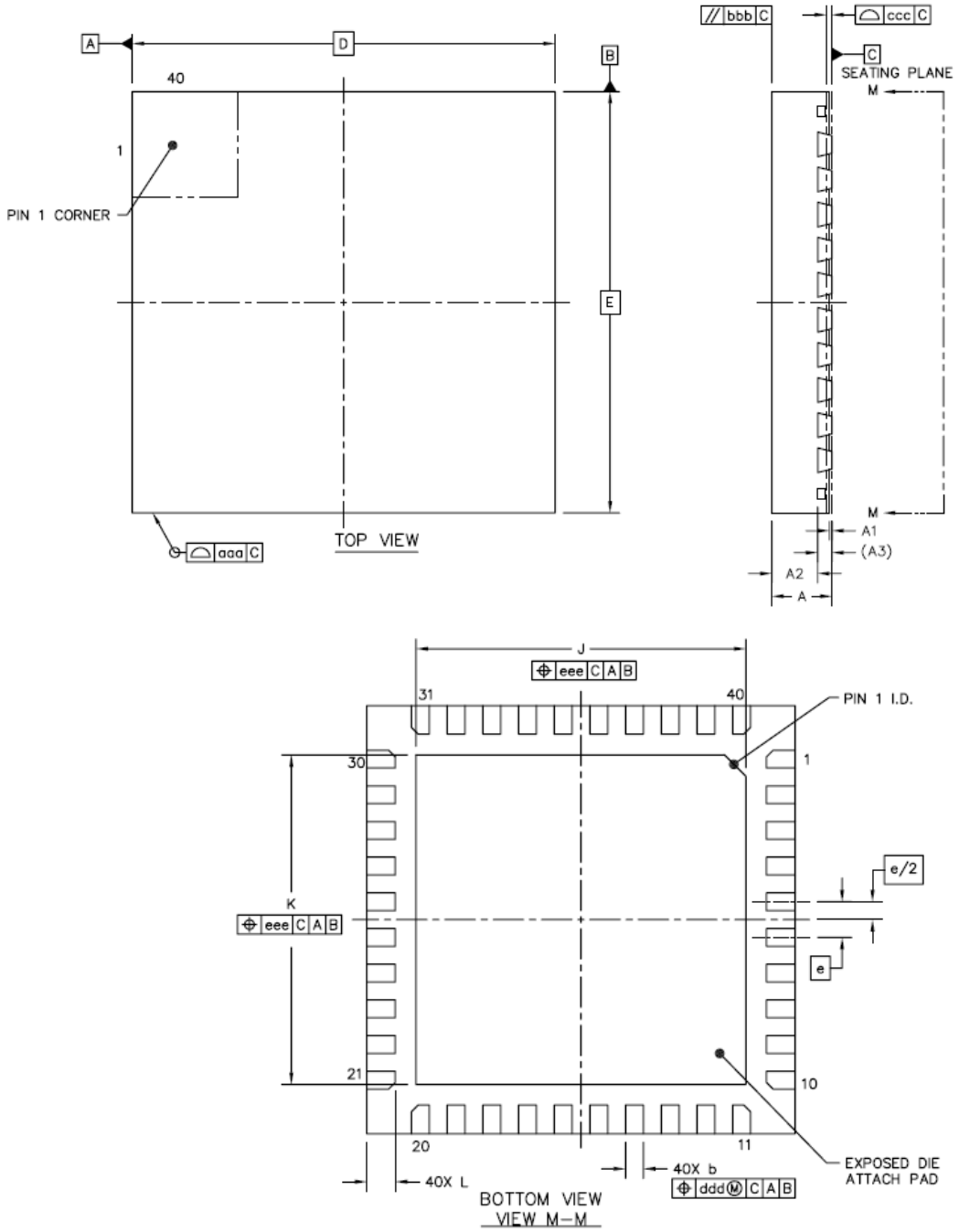
Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x1B	TXNTRIG	r	r	r	PENDACK	INDIRECT	TXNACKREQ	TXNSEC EN	TXNTRIG	0000 0000
0x24	TXSR	TXRETRY1	TXRETRY 0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS	0000 0000
0x2C	SECCR0	SECIGNOR E	SECSTAR T	RXCIPHER2	RXCIPHER1	RXCIPHER0	TXNCIPHER2	TXNCIPH ER1	TXNCIPHE R0	0000 0000
0x30	RXSR	RXFFFULL	WRFF1	UPSECERR	RXFFOVFL	RXCRCERR	SECDECERR	r	r	0000 0000
0x31	ISRSTS	SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF	0000 0000
0x37	SECCR2	UPDEC	UPENC	TXG2CIPHE R2	TXG2CIPHER 1	TXG2CIPHER 0	TXG1CIPHER 2	TXG1CIP HER1	TXG1CIPH ER0	0000 0000
0x240	UPNONCE_0	UPNONCE[7:0]								0000 0000
0x241	UPNONCE_1	UPNONCE[15:8]								0000 0000
0x242	UPNONCE_2	UPNONCE[23:16]								0000 0000
0x243	UPNONCE_3	UPNONCE[31:24]								0000 0000
0x244	UPNONCE_4	UPNONCE[39:32]								0000 0000
0x245	UPNONCE_5	UPNONCE[47:40]								0000 0000
0x246	UPNONCE_6	UPNONCE[55:48]								0000 0000
0x247	UPNONCE_7	UPNONCE[63:56]								0000 0000
0x248	UPNONCE_8	UPNONCE[71:64]								0000 0000
0x249	UPNONCE_9	UPNONCE[79:72]								0000 0000
0x24A	UPNONCE_10	UPNONCE[81:80]								0000 0000
0x24B	UPNONCE_11	UPNONCE[95:88]								0000 0000
0x24C	UPNONCE_12	UPNONCE[89:96]								0000 0000

5. Package Information

5.1. Package Drawing

The QFN-40 package outline is given below.

QFN-40, 6x6mm²



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	4.52	4.62	4.72
	Y	K	4.52	4.62	4.72
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

5.2. Package Soldering

5.2.1. Background

The UZ2400 is housed in a small 40-pin lead-free QFN 6x6 mm^2 package. The packaged part passes the Level 3 pre-condition testing.

5.2.2. Reference Reflow Temperature Curve

Figure 30 shows a reference temperature curve of the SMD package IR reflow. Different equipments may have different optimized reflow conditions. The user may need to modify the reflow profile to suit the particular equipment used in order to maximize the yield.

Pb-free SMD Package IR Reflow Profile

Step#	Profile Feature	Condition / Duration
Step 1	Ramp-up rate	1.5-3℃ /sec
Step 2	Preheat : 150~ 200℃ (Ta-Tb)	t1-t2: 60~80 sec
Step 3	Ramp-up rate (T_L to T_P)	1.5-3℃ /sec
	Temperature maintained above 220℃ (T_L)	t_L : 80~150 sec
Step 4	Peak temperature (T_P)	260+0/-5℃
	Time within 5℃ of actual peak temperature	30±10 sec
Step 5	Ramp-down rate	6℃/sec. Max.

Note: 1. Time 25℃ to peak temperature: 8 minutes max.
2. The time between reflows shall be 5 minutes minimum and 60 minutes maximum.

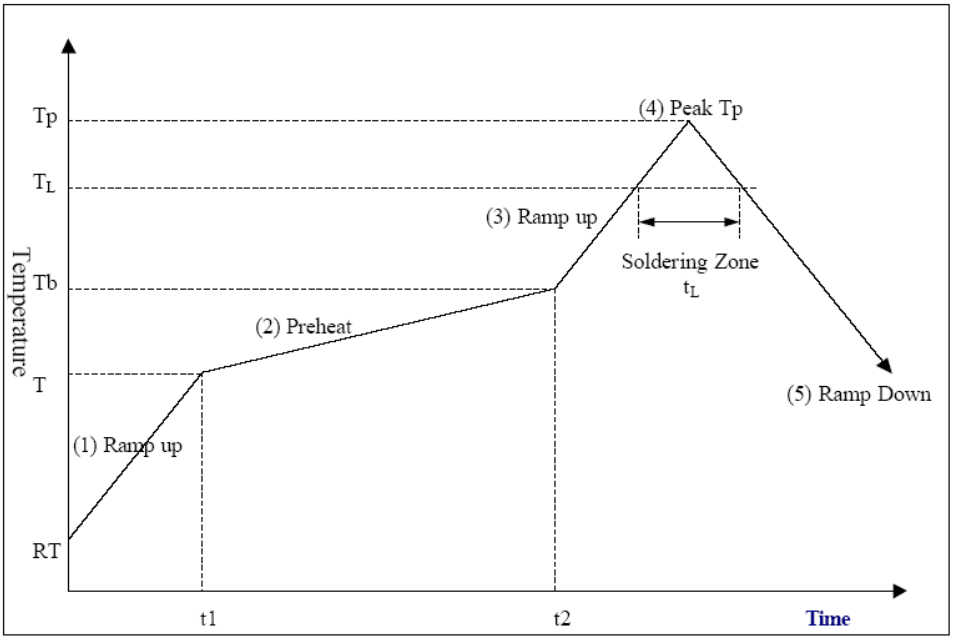


Figure 30: Reference SMD package IR reflow profile

Appendix A. Typical Characteristics

Data Rate=250kbps, T_A=25°C, unless otherwise specified

A.1 Output Power

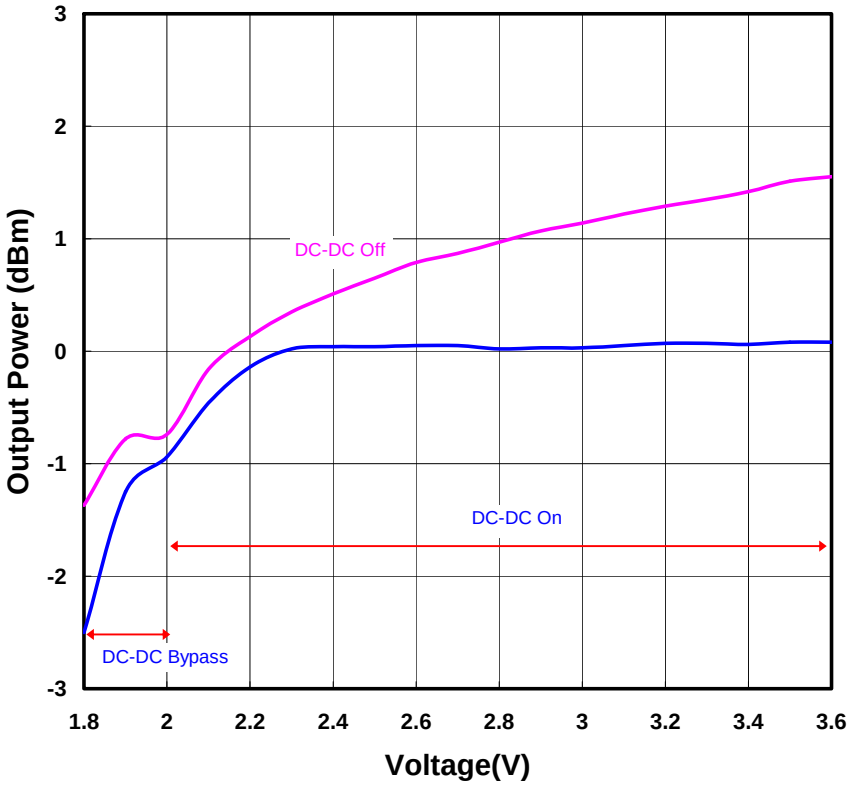


Figure A-1: Output power vs. supplied voltage at 2445MHz.

The lower blue line shown in Figure A-1 combines with two operation conditions. When the bias voltage is higher than 2.0V, the characteristic output power curve is obtained with DC-DC converter turned on which corresponds with the following register settings (LREG0x250=0x17, LREG0x273=0x80 and LREG0x274=0xC0). When the bias drops to below 2.0V the converter enters into the BYPASS mode with the following register settings (LREG0x250=0x07, LREG0x273=0x9F and LREG0x274=0xC0).

The upper pink line combines with two operation conditions as well. When the bias voltage is higher than 2.0V, the characteristic output power curve is obtained with LREG0x250=0x07, LREG0x273=0x80 and LREG0x274=0xE5. When the bias drops to below 2.0V the register settings change to LREG0x250=0x07, LREG0x273=0x9F and LREG0x274=0xC0.

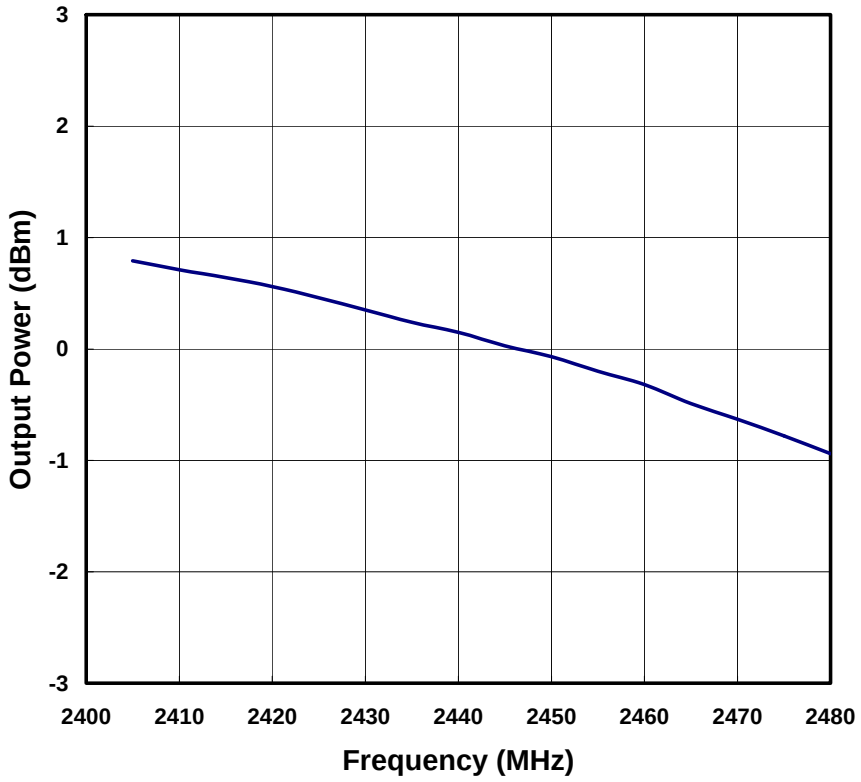


Figure A-2: Output power vs. channel frequency at VDD=3V with DC-DC on.

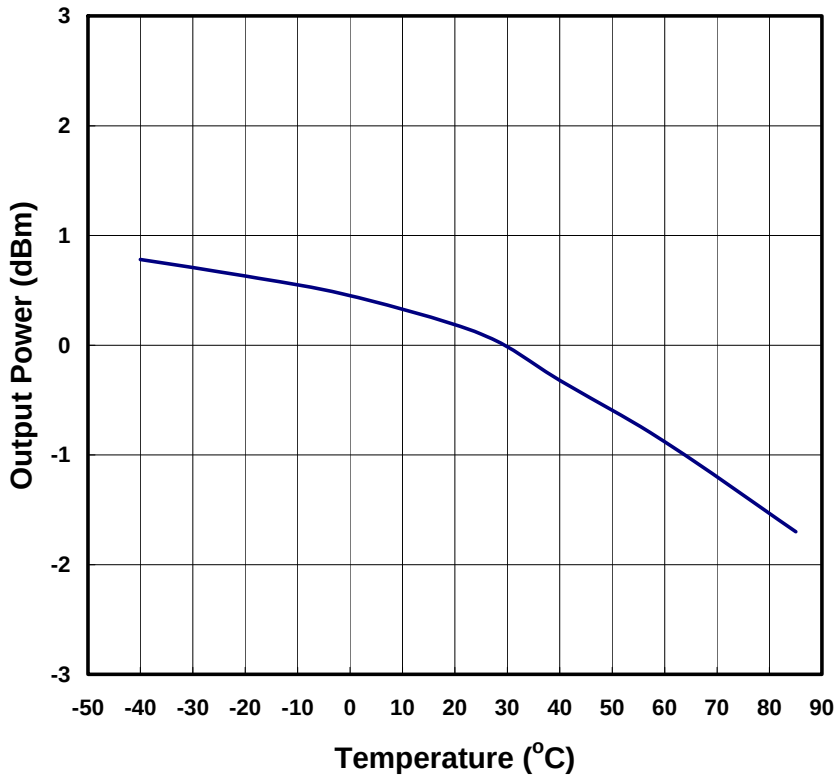


Figure A-3: Output power vs. temperature at 2445MHz and VDD=3V with DC-DC on.

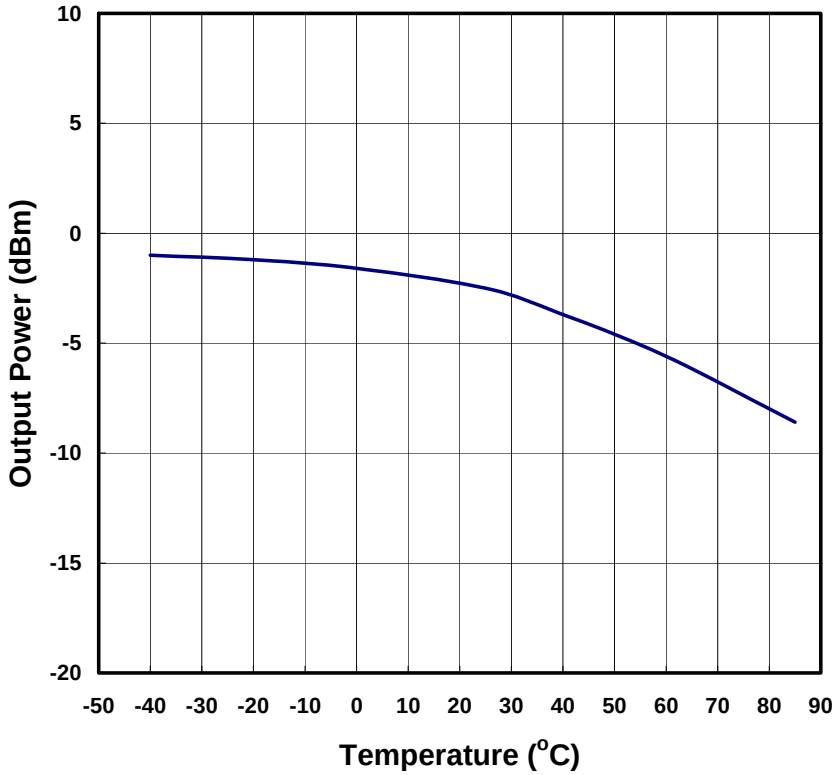


Figure A-4: Output power vs. temperature at 2445MHz and VDD=1.8V with DC-DC Bypass.

A.2 Sensitivity

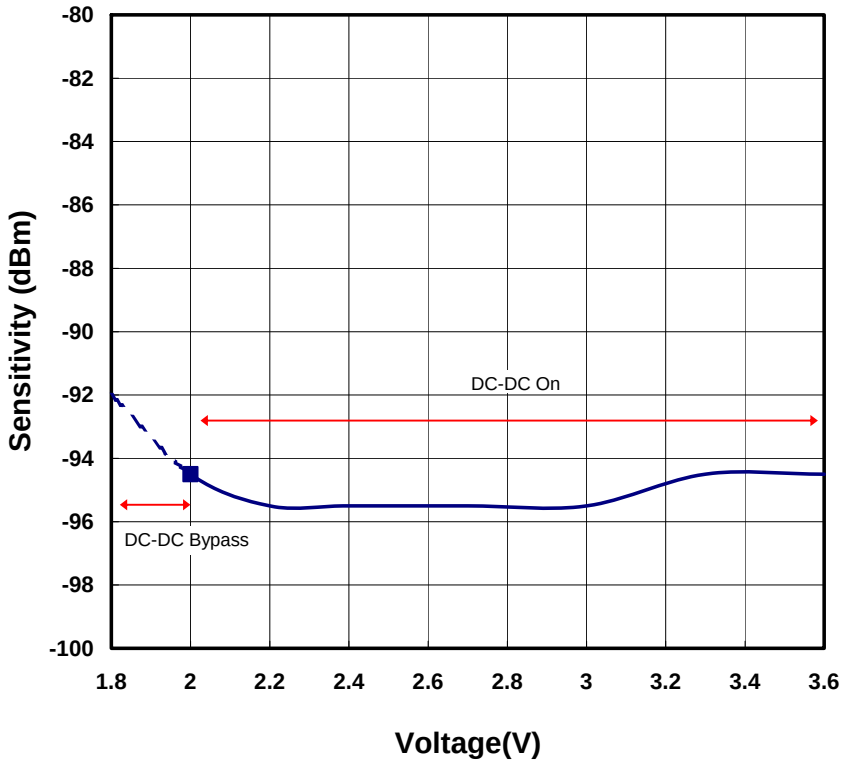


Figure A-5: Sensitivity vs. supply voltage at 2445MHz

When the bias voltage is higher than 2.0V, the characteristic sensitivity curve is obtained with DC-DC converter turned on which corresponds with the following register settings (LREG0x250=0x17, LREG0x273=0x80 and LREG0x274=0xC0). When the bias drops to below 2.0V the converter enters into the BYPASS mode with the following register settings (LREG0x250=0x07, LREG0x273=0x9F and LREG0x274=0xC0).

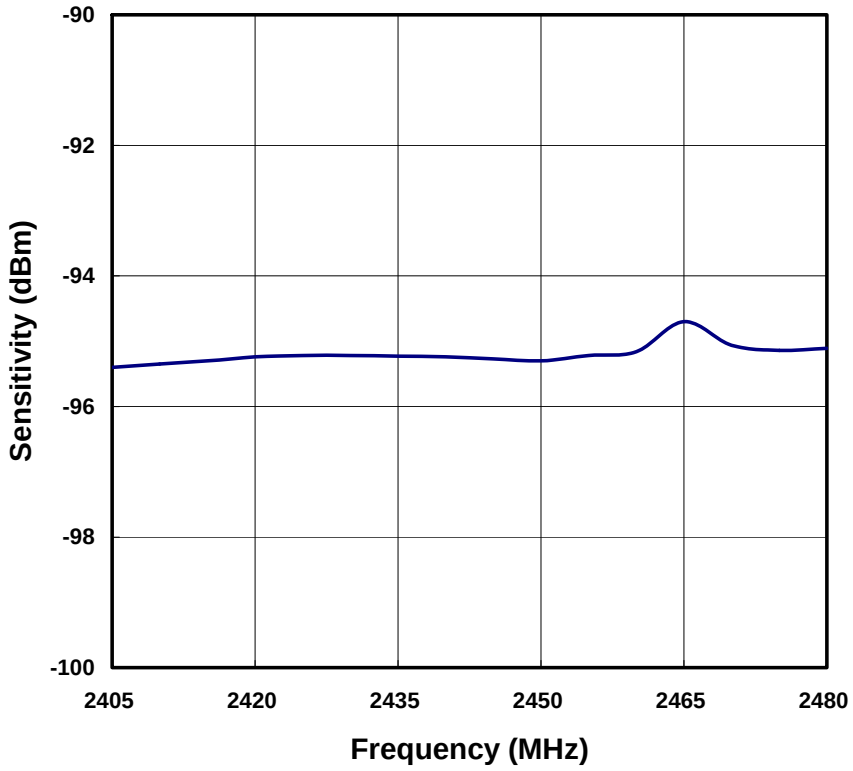


Figure A-6: Sensitivity vs. channel frequency at VDD=3V with DC-DC on.

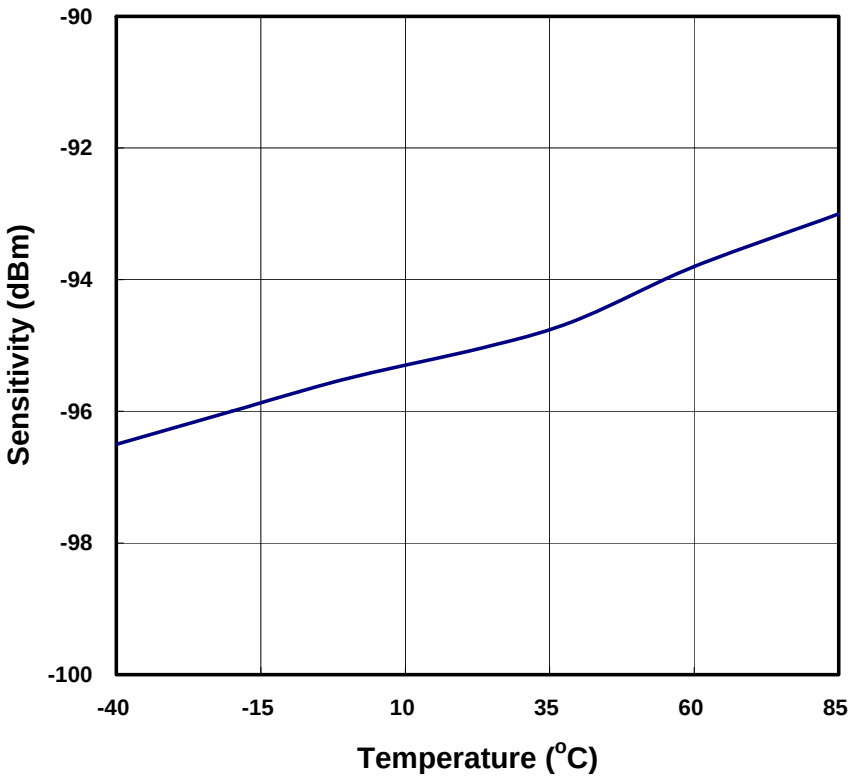


Figure A-7: Sensitivity vs. temperature at 2445MHz and VDD=3V with DC-DC on.

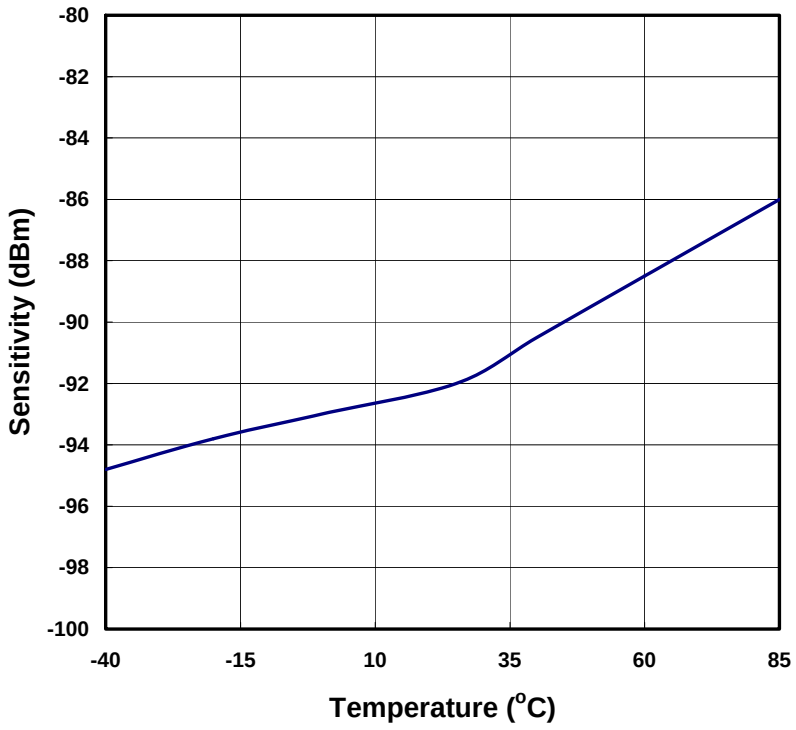


Figure A-8: Sensitivity vs. temperature at 2445MHz and VDD=1.8V with DC-DC Bypass.

Appendix B. TX Power Configuration

Default output power is 0dBm. Different output power settings are listed in the table below.

TX Output Power Register Control			
LREG0x253[3:0]: PA 1 Control (Fine-tuning)	LREG0x274[7:4]: PA 1 Control (Coarse-tuning) LREG0x274[3:0]: PA 2 Control	LREG0x203[7:3] TX Gain Control in dB	TX Output Power
00	C0 (Vdd=1.8V~2.0V) C5 (Vdd=2.0V~3.6V)	00000	0 dBm
		00001	-0.1 dBm
		00010	-0.3 dBm
		00011	-0.6 dBm
		00100	-0.9 dBm
		00101	-1.1 dBm
		00110	-1.2 dBm
		00111	-1.3 dBm
		01000	-1.4 dBm
		01001	-1.5 dBm
		01010	-1.7 dBm
		01011	-2.0 dBm
		01100	-2.2 dBm
		01101	-2.4 dBm
		01110	-2.6 dBm
		01111	-2.8 dBm
		10000	-3.1 dBm
		10001	-3.3 dBm
		10010	-3.6 dBm
		10011	-3.8 dBm
		10100	-4.2 dBm
		10101	-4.4 dBm
		10110	-4.7 dBm
		10111	-5.0 dBm
		11000	-5.3 dBm
		11001	-5.7 dBm
		11010	-6.2 dBm
		11011	-6.5 dBm
		11100	-6.9 dBm
		11101	-7.4 dBm
		11110	-7.9 dBm
		11111	-8.3 dBm
0C	81	11111	-16 dBm
0C	09	11111	-24 dBm
09	01	11111	-32 dBm
08	01	11111	-40 dBm

Note: Gain resolution is variable between different chips. Gain step of LREG0x203[7:3] is monotonic and nonlinear with gain resolution of 0.1 ~ 0.5 dB.

Appendix C. Register Descriptions

Register Types

Register Type	Description
R/W	Read/Write register
R/W1C	Read/Write '1' to clear register
R	Read-only register
RC	Read to clear register
W	Write-only register
WT	Write 1 to trigger register, automatically cleared by hardware

C.1 Short Registers (SREG0x00~SREG0x3F)

0x00	RXMCR	0x10	ORDER	0x20	ESLOTG6	0x30	RXSR
0x01	PANIDL	0x11	TXMCR	0x21	TXPEND	0x31	ISRSTS
0x02	PANIDH	0x12	Reserved	0x22	WAKECTL	0x32	INTMSK
0x03	SADRL	0x13	ESLOTG1C	0x23	ALIGNOFF	0x33	LRXSR
0x04	SADRH	0x14	Reserved	0x24	TXSR	0x34	SPIRXF
0x05	EADR_0	0x15	TXCON	0x25	TXBCNMSK	0x35	SLPACK
0x06	EADR_1	0x16	PACON0	0x26	GATECLK	0x36	RFCTL
0x07	EADR_2	0x17	PACON1	0x27	Reserved	0x37	SECCR2
0x08	EADR_3	0x18	FIFOEN	0x28	MACTMRL	0x38	BBREG0
0x09	EADR_4	0x19	Reserved	0x29	MACTMRH	0x39	Reserved
0x0A	EADR_5	0x1A	TXBTRIG	0x2A	SOFTRST	0x3A	BBREG2
0x0B	EADR_6	0x1B	TXNTRIG	0x2B	Reserved	0x3B	BBREG3
0x0C	EADR_7	0x1C	TXG1TRIG	0x2C	SECCR0	0x3C	BBREG4
0x0D	RXFLUSH	0x1D	TXG2TRIG	0x2D	SECCR1	0x3D	BBREG5
0x0E	Reserved	0x1E	ESLOTG23	0x2E	TXPEMISP	0x3E	BBREG6
0x0F	Reserved	0x1F	ESLOTG45	0x2F	Reserved	0x3F	BBREG7

SREG0x00: RXMCR

RECEIVE MAC CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	NOACKRSP	r	PANCOORD	COORD	r	r
R-0	R-0	R/W-0	R-0	R/W-0	R/W-0	R-0	R-0

Bit 7-6 **Reserved**: Maintain as '0b00'

Bit 5 **NOACKRSP**: Automatic Acknowledgement Response
- 0: (default) Enables automatic acknowledgement response
- 1: Disables automatic acknowledgement response

Bit 4 **Reserved**: Maintain as '0b0'

Bit 3 **PANCOORD**: PAN Coordinator
- 0: (default) Device is not set as PAN coordinator
- 1: Set device as PAN coordinator

Bit 2 **COORD**: Coordinator
- 0: (default) Device is not set as coordinator
- 1: Set device as coordinator

Bit 1-0 **Reserved**: Maintain as '0b00'

SREG0x01: PANIDL

PAN ID LOW BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PANID7	PANID6	PANID5	PANID4	PANID3	PANID2	PANID1	PANID0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **PANID[7:0]**: PAN identifier of this device, Low Byte

SREG0x02: PANIDH

PAN ID HIGH BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PANID15	PANID14	PANID13	PANID12	PANID11	PANID10	PANID9	PANID8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **PANID[15:8]**: PAN identifier of this device, High Byte

SREG0x03: SADRL

SHORT ADDRESS LOW BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SADR7	SADR6	SADR5	SADR4	SADR3	SADR2	SADR1	SADR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SADR[7:0]**: 16-bit Short Address of this device, Low Byte

SREG0x04: SADRH

SHORT ADDRESS HIGH BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SADR15	SADR14	SADR13	SADR12	SADR11	SADR10	SADR9	SADR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SADR[15:8]**: 16-bit Short Address of this device, High Byte

SREG0x05: EADR_0

EXTENDED ADDRESS 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR7	EADR6	EADR5	EADR4	EADR3	EADR2	EADR1	EADR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **EADR[7:0]**: 64-Bit Extended Address of this device

SREG0x06: EADR_1

EXTENDED ADDRESS 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR15	EADR14	EADR13	EADR12	EADR11	EADR10	EADR9	EADR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **EADR[15:8]**: 64-Bit Extended Address of this device

SREG0x07: EADR_2

EXTENDED ADDRESS 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR23	EADR22	EADR21	EADR20	EADR19	EADR18	EADR17	EADR16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **EADR[23:16]**: 64-Bit Extended Address of this device

SREG0x08: EADR_3

EXTENDED ADDRESS 3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR31	EADR30	EADR29	EADR28	EADR27	EADR26	EADR25	EADR24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **EADR[31:24]**: 64-Bit Extended Address of this device

SREG0x09: EADR_4

EXTENDED ADDRESS 4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR39	EADR38	EADR37	EADR36	EADR35	EADR34	EADR33	EADR32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **EADR[39:32]**: 64-Bit Extended Address of this device

SREG0x0A: EADR_5

EXTENDED ADDRESS 5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR47	EADR46	EADR45	EADR44	EADR43	EADR42	EADR41	EADR40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **EADR[47:40]**: 64-Bit Extended Address of this device

SREG0x0B: EADR_6

EXTENDED ADDRESS 6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR55	EADR54	EADR53	EADR52	EADR51	EADR50	EADR49	EADR48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **EADR[55:48]**: 64-Bit Extended Address of this device

SREG0x0C: EADR_7

EXTENDED ADDRESS 7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR63	EADR62	EADR61	EADR60	EADR59	EADR58	EADR57	EADR56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **EADR[63:56]**: 64-Bit Extended Address of this device

SREG0x0D: RXFLUSH

RECEIVE FIFO FLUSH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	WAKEPOL	WAKEPAD	r	NOCSMATXN	r	r	RXFLUSH
R-0	R/W-1	R/W-1	R-0	R/W-0	R-0	R-0	WT-0

Bit 7 **Reserved**: Maintain as '0b0'

Bit 6 **WAKEPOL**: WAKE Signal Polarity
0: WAKE signal polarity is active-low
1: (default) WAKE signal polarity is active-high

Bit 5 **WAKEPAD**: WAKE Pin Enable
0: Enable WAKE pin
1: (default) Disable WAKE pin

Bit 4 **Reserved**: Maintain as '0b0'

Bit 3 **NOCSMAN**: Carrier Sense Multiple Access with Collision Avoidance (CSMA-CA) for TX Normal FIFO
0: (default) Enable CSMA-CA for TX normal FIFO
1: Disable CSMA-CA for TX normal FIFO

Bit 2-1 **Reserved**: Maintain as '0b00'

Bit 0 **RXFLUSH**: Flush the RX FIFO
1: Flush RX FIFO. RX FIFO data is not modified. If Ping-pong FIFO is enabled (SREG0x34[0]=1), both FIFOs are flushed at the same time. Bit is automatically cleared to '0' by hardware.

SREG0x10: ORDER

BEACON AND SUPERFRAME ORDER							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
BO3	BO2	BO1	BO0	SO3	SO2	SO1	SO0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 7-4 **BO[3:0]**: Beacon Order (macBeaconOrder) (1)
Specifies how often the coordinator will transmit a beacon. (2)
0000: 0
…
1110: 14
1111: (default) The coordinator will not transmit a beacon and the Superframe Order (SO) parameter value is ignored

Bit 3-0 **SO[3:0]**: Superframe Order (macSuperframeOrder)(1)
Specifies the length of the active portion of the superframe, including the beacon frame. (2)
0000: 0
…
1110: 14
1111: (default) The superframe will not be active following the beacon. (i.e., no active portion in the superframe)

Note 1: Refer to IEEE 802.15.4™-2006 Standard, Section 7.5.1.1 "Superframe Structure".
2: PANs that wish to use the superframe structure shall set macBeaconOrder to a value between 0 and 14 and macSuperframeOrder to a value between 0 and the value of macBeaconOrder (i.e., $0 \leq SO \leq BO \leq 14$).

SREG0x11: TXMCR

CSMA-CA MODE CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
NOCSMAG	r	SLOTTED	MACMINBE1	MACMINBE0	CSMABF2	CSMABF1	CSMABF0
R/W-0	R-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0

Bit 7 **NOCSMAG**: Carrier Sense Multiple Access with Collision Avoidance (CSMA-CA) for TX GTS FIFO
0: (default) Enable CSMA-CA for TX GTS FIFO
1: Disable CSMA-CA for TX GTS FIFO

Bit 6 **Reserved**: Maintain as '0b0'

Bit 5 **SLOTTED**: Slotted CSMA-CA Mode
0: (default) Disable Slotted CSMA-CA mode
1: Enable Slotted CSMA-CA mode

Bit 4-3 **MACMINBE[1:0]**: MAC Minimum Backoff Exponent (macMinBE)
The minimum value of the backoff exponent in the CSMA-CA algorithm
00: Collision avoidance is disabled (1)
01: 1
10: 2
11: 3 (default)

Bit 2-0 **CSMABF[2:0]**: CSMA Backoff (macMaxCSMABackoff)
The maximum number of backoffs the CSMA-CA algorithm will attempt before declaring a channel access failure. (1)
000: 0
001: 1
010: 2
011: 3
100: 4 (default)
101: 5
110: Undefined
111: Undefined

Note 1: Please refer to IEEE802.15.4TM-2006, Table 86 – MAC PIB attributes

SREG0x13: ESLOTG1C

END SLOT OF GTS1 AND CAP							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
GTS1-3	GTS1-2	GTS1-1	GTS1-0	CAP3	CAP2	CAP1	CAP0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-4 **GTS1[3:0]**: End Slot of 1st GTS
0000: 0 (default)
…
1111: 15

Bit 3-0 **CAP[3:0]**: End Slot of Contention Access Period (CAP)
0000: 0 (default)
…
1111: 15

SREG0x15: TXCON

TX CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXONT6	TXONT5	TXONT4	TXONT3	TXONT2	TXONT1	TXONT0	r
R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R-1

Bit 7-1 **TXONT[6:0]**: TX Settling Time 0
Transmitter settling time to begin packet transmission. TXONT is a 9-bit value. TXONT[8:7] bits are located in SREG0x18[1:0].
0101000: (default - Do Not Change)

Bit 0 **Reserved**: Maintain as '0b1'

SREG0x16: PACON0

POWER AMPLIFIER CONTROL 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PACONT7	PACONT6	PACONT5	PACONT4	PACONT3	PACONT2	PACONT1	PACONT0
R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1

Bit 7-0 **PACONT[7:0]**: Power Amplifier Settling Time 0
Power amplifier settling time to begin packet transmission. PACONT is a 9-bit value. The PACONT8 bit is located in SREG0x17[0].
00101001: (default - Do Not Change)

SREG0x17: PACON1

POWER AMPLIFIER CONTROL 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	PAONTS3	PAONTS2	PAONTS1	PAONTS0	PACONT8
R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0

Bit 7-5 **Reserved**: Maintain as '0b000'

Bit 4-1 **PAONTS[3:0]**: Power Amplifier Settling Time 1
Power amplifier settling time to begin packet transmission.
0001: (default)
0100: (optimized - Do Not Change)

Bit 0 **PACONT[8]**: Power Amplifier Settling Time 0
Power amplifier settling time to begin packet transmission. PACONT is a 9-bit value. The PACONT[7:0] bits are located in SREG0x16[7:0].
0: (default - Do Not Change)

SREG0x18: FIFOEN

FIFO ENABLE AND TX CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
FIFOEN	r	TXONTS3	TXONTS2	TXONTS1	TXONTS0	TXONT8	TXONT7
R/W-1	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0

Bit 7 **FIFOEN**: FIFO Enable
1: (default - Do Not Change) Enable

Bit 6 **Reserved**: Maintain as '0b0'

Bit 5-2 **TXONTS[3:0]**: TX Settling Time 1
Transmitter settling time to begin packet transmission.
0010: (default)
0101: (optimized - Do Not Change)

Bit 1-0 **TXONT[8:7]**: TX Settling Time 0
Transmitter settling time to begin packet transmission. TXONT is a 9-bit value. TXONT[6:0] bits are located in SREG0x15[7:1].
00: (default - Do Not Change)

SREG0x1A: TXBTRIG

TRANSMIT BEACON FIFO CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	r	TXBCNSECEN	TXBCNTRIG
R-0	R-0	R-0	R-0	R-0	R-0	R/W-0	WT-0

Bit 7-2 **Reserved**: Maintain as '0b000000'

Bit 1 **TXBSECEN**: TX Beacon FIFO Security Enabled bit

0: (default) Security disabled

1: Security enabled

Bit 0 **TXBCNTRIG**: Transmit Frame in TX Beacon FIFO bit

1: Transmit the frame in the TX Beacon FIFO; bit is automatically cleared by hardware.

SREG0x1B: TXNTRIG

TRANSMIT NORMAL FIFO CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG
R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	WT-0

Bit 7-5 **Reserved**: Maintain as '0b000'

Bit 4 **PENDACK:** Frame Pending Status bit (1)

Status of the frame pending bit in the received Acknowledgement frame.

0: (default) Frame pending bit = 0

1: Frame pending bit = 1

Bit 3 **INDIRECT:** Activate Indirect Transmission bit (coordinator only)

0: (default) Indirect transmission disabled

1: Indirect transmission enabled

Bit 2 **TXNACKREQ:** TX Normal FIFO Acknowledgement Request bit (2)

Transmit a packet with Acknowledgement request. If Acknowledgement is not received, the UZ2400 retransmits up to 3 times.

0: (default) No Acknowledgement packet requested

1: Acknowledgement packet requested

Bit 1 **TXNSECEN:** TX Normal FIFO Security Enabled bit (3)

0: (default) Security disabled

1: Security enabled

Bit 0 **TXNTRIG:** Transmit Frame in TX Normal FIFO bit

1: Transmit the frame in the TX Normal FIFO. Bit is automatically cleared to '0' by hardware.

Note 1: Refer to IEEE 802.15.4™-2006 Standard, Section 7.2.1.1.3 "Frame Pending Subfield".

2: Refer to IEEE 802.15.4™-2006 Standard, Section 7.2.1.1.4 "Acknowledgement Request Subfield".

3: Refer to IEEE 802.15.4™-2006 Standard, Section 7.2.1.1.2 "Security Enabled Subfield".

SREG0x1C: TXG1TRIG

GTS1 FIFO CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXG1IFETRY1	TXG1IFETRY0	TXG1SLOT2	TXG1SLOT1	TXG1SLOT0	TXG1ACKREQ	TXG1SECEN	TXG1TRIG
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	WT-0

Bit 7-6 **TXG1IFETRY[1:0]**: GTS1 FIFO Retry Times
Write: Limited retry times of the packet
Read: Number of retry times of the successfully transmitted packet
00: 0 (default)
…
11: 3

Bit 5-3 **TXG1SLOT[2:0]**: GTS Slot that GTS1 FIFO Occupies
000: 0 (default)
…
111: 7

Bit 2 **TXG1ACKREQ**: TX GTS1 FIFO Acknowledgement Request
Transmit a packet with Acknowledgement request. If Acknowledgement is not received, the UZ2400 retransmits up to the times set by SREG0x1C[7:6].
0: (default) Acknowledgement Request disabled
1: Acknowledgement Request enabled

Bit 1 **TXG1SECEN**: TX GTS1 FIFO Security Enabled
0: (default) Security disabled
1: Security enabled

Bit 0 **TXG1TRIG**: Transmit Frame in TX GTS1 FIFO
1: Transmit the frame in the TX GTS1 FIFO. Bit is automatically cleared to '0' by hardware.

SREG0x1D: TXG2TRIG

GTS2 FIFO CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXG2IFETRY1	TXG2IFETRY0	TXG2SLOT2	TXG2SLOT1	TXG2SLOT0	TXG2ACKREQ	TXG2SECEN	TXG2TRIG
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	WT-0

Bit 7-6 **TXG2IFETRY[1:0]**: GTS2 FIFO Retry Times
Write: Limited retry times of the packet
Read: Number of retry times of the successfully transmitted packet
00: 0 (default)
…
11: 3

Bit 5-3 **TXG2SLOT[2:0]**: GTS Slot that GTS2 FIFO Occupies
000: 0 (default)
…
111: 7

Bit 2 **TXG2ACKREQ**: TX GTS2 FIFO Acknowledgement Request
Transmit a packet with Acknowledgement request. If Acknowledgement is not received, the UZ2400 retransmits up to the times set by SREG0x1D[7:6].
0: (default) Acknowledgement Request disabled
1: Acknowledgement Request enabled

Bit 1 **TXG2SECEN**: TX GTS2 FIFO Security Enabled
0: (default) Security disabled
1: Security enabled

Bit 0 **TXG2TRIG**: Transmit Frame in TX GTS2 FIFO
1: Transmit the frame in the TX GTS2 FIFO. Bit is automatically cleared to '0' by hardware.

SREG0x1E: ESLOTG23

END SLOT OF GTS3 AND GTS2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
GTS3-3	GTS3-2	GTS3-1	GTS3-0	GTS2-3	GTS2-2	GTS2-1	GTS2-0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-4 **GTS3[3:0]**: End Slot of 3rd GTS
0000: 0 (default)
…
1111: 15

Bit 3-0 **GTS2[3:0]**: End Slot of 2nd GTS
0000: 0 (default)
…
1111: 15

SREG0x1F: ESLOTG45

END SLOT OF GTS5 AND GTS4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
GTS5-3	GTS5-2	GTS5-1	GTS5-0	GTS4-3	GTS4-2	GTS4-1	GTS4-0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-4 **GTS5[3:0]**: End Slot of 5th GTS
0000: 0 (default)
…
1111: 15

Bit 3-0 **GTS4[3:0]**: End Slot of 4th GTS
0000: 0 (default)
…
1111: 15

SREG0x20: ESLOTG6

END SLOT OF GTS6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	GTS6-3	GTS6-2	GTS6-1	GTS6-0
R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-4 **Reserved**: Maintain as '0b0000'

Bit 3-0 **GTS6[3:0]**: End Slot of 6th GTS (1)
0000: 0 (default)
…
1111: 15

Note 1: If 7th GTS exists, the end slot must be 15

SREG0x21: TXPEND

TX DATA PENDING							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	r	GTSSWITCH	r
R-1	R-0	R-0	R-0	R-0	R-1	R/W-0	R-0

Bit 7-2 **Reserved**: Maintain as '0b100001'

Bit 1 **GTSSWITCH**: Continue TX GTS FIFO Switch

0: (default) GTS1 and GTS2 FIFO will stop toggling with each other if the transmission fails

1: GTS1 and GTS2 FIFO will toggle with each other

Bit 0 **Reserved**: Maintain as '0b0'

SREG0x22: WAKECTL

WAKE CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
IMMWAKE	REGWAKE	INTL5	INTL4	INTL3	INTL2	INTL1	INTL0
R/W-0	WT-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 **IMMWAKE**: Immediate Wake-up Mode Enable
0: (default) Disable Immediate Wake-up mode
1: Enable Immediate Wake-up mode

Bit 6 **REGWAKE**: Register Triggered Wake-up Signal
1: To wake UZ2400 up. Bit is automatically cleared to '0' by hardware.

Bit 5-0 **INTL[5:0]**: Interval to Start Beacon
The timing interval between slotted mode triggered (set by SREG0x10[7:4]) and the first time to send beacon frame.
000000: 0 (default)
000011: 3 (optimized - Do Not Change)

SREG0x23: ALIGNOFF

ALIGN OFFSET							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
AOFFSET7	AOFFSET6	AOFFSET5	AOFFSET4	AOFFSET3	AOFFSET2	AOFFSET1	AOFFSET0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **AOFFSET[7:0]**: Offset to Align Beacon Boundary

Superframe counter offset to align with beacon boundary. Alignment will happen whenever a beacon is received. Only for device mode.

00000000: (default)

00010101: (optimized - Do Not Change)

SREG0x24: TXSR

TX STATUS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXRETRY1	TXRETRY0	CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-6 **TXRETRY[1:0]**: TX Normal FIFO Retry Times
Number of retrys of the most recent TX Normal FIFO transmission.
00: 0 (default)
…
11: 3

Bit 5 **CCAFAIL**: Clear Channel Assessment (CCA) Status of Last Transmission
0: (default) Channel Idle
1: Channel busy

Bit 4 **TXG2FNT**: GTS2 FIFO Transmission Status
0: (default) Succeeded
1: Fail, no enough time to transmit before the end of a GTS.

Bit 3 **TXG1FNT**: GTS1 FIFO Transmission Status
0: (default) Succeeded
1: Fail, no enough time to transmit before the end of a GTS.

Bit 2 **TXG2S**: GTS2 FIFO Release Status
0: (default) Succeeded
1: Fail, retry count exceed

Bit 1 **TXG1S**: GTS1 FIFO Release Status
0: (default) Succeeded
1: Fail, retry count exceed

Bit 0 **TXNS**: Normal FIFO Release Status
0: (default) Succeeded
1: Fail, retry count exceed

SREG0x25: TXBCNMSK

TRANSMIT BEACON CONTROL MASK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXBCNMSK	r	r	r	r	r	r	r
R/W-0	R-0	R-1	R-1	R-0	R-0	R-0	R-0

Bit 7 **TXBCNMSK**: TX Beacon FIFO Interrupt Mask
0: (default) Enable TX Beacon FIFO interrupt
1: Disable TX Beacon FIFO interrupt.

Bit 6-0 **Reserved**: Maintain as '0b0110000'

SREG0x26: GATECLK

GATED CLOCK CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	SPISYNC	ENRXM	ENGTS	ENTXM	r	r
R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0

Bit 7-6 **Reserved**: Maintain as '0b00'

Bit 5 **SPISYNC**: SPI Interface Synchronization
- 0: (default) Disable
- 1: (optimized - Do Not Change) Enable

Bit 4 **ENRXM**: RX MAC Clock Enable
- 0: (default) Disable
- 1: Enable

Bit 3 **ENGTS**: GTS FIFO Clock
- 0: (default) Disable
- 1: Enable

Bit 2 **ENTXM**: TX MAC Clock Enable
- 0: (default) Disable
- 1: Enable

Bit 1-0 **Reserved**: Maintain as '0b00'

SREG0x28: MACTMRL

MAC TIMER LOW BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
MACTMR7	MACTMR6	MACTMR5	MACTMR4	MACTMR3	MACTMR2	MACTMR1	MACTMR0
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

Bit 7-0 **MACTMR[7:0]**: 16-Bit MAC Timer, Low Byte

SREG0x29: MACTMRH

MAC TIMER HIGH BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
MACTMR15	MACTMR14	MACTMR13	MACTMR12	MACTMR11	MACTMR10	MACTMR9	MACTMR8
WT-0	WT-0	WT-0	WT-0	WT-0	WT-0	WT-0	WT-0

Bit 7-0 **MACTMR[15:8]**: 16-Bit MAC Timer, High Byte
Unit: 8μs
Writing SREG0x29 will trigger MAC timer (SREG0x29:SREG0x28) to count down.

SREG0x2A: SOFTRST

SOFTWARE RESET							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	RSTPWR	RSTBB	RSTMAC
R-0	R-0	R-0	R-0	R-0	WT-0	WT-0	WT-0

Bit 7-3 **Reserved**: Maintain as '0b00000'

Bit 2 **RSTPWR**: Power Management Reset

1: Reset power management circuitry. Initialization is not needed after **RSTPWR** reset. Bit is automatically cleared to '0' by hardware.

Bit 1 **RSTBB**: Baseband Reset

1: Reset baseband circuitry. Initialization is not needed after **RSTBB** reset. Bit is automatically cleared to '0' by hardware.

Bit 0 **RSTMAC**: MAC and Short/Long Address Registers Reset

1: Reset MAC circuitry and Short/Long Address Registers. Initialization is needed after **RSTMAC** reset. Bit is automatically cleared to '0' by hardware.

SREG0x2C: SECCR0

SECURITY CONTROL 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SECIGNORE	SECSTART	RXCIPHER2	RXCIPHER1	RXCIPHER0	TXNCIPHER2	TXNCIPHER1	TXNCIPHER0
WT-0	WT-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 **SECIGNORE**: RX Security Decryption Ignore
1: Ignore decryption process. Bit is automatically cleared to '0' by hardware.

Bit 6 **SECSTART**: RX Security Decryption Start
1: Start decryption process. Bit is automatically cleared to '0' by hardware.

Bit 5-3 **RXCIPHER[2:0]**: RX FIFO Security Suite Select
000: (default) Undefined
001: AES-ENC
010: AES-ENC-MIC-128
011: AES-ENC-MIC-64
100: AES-ENC-MIC-32
101: AES-MIC-128
110: AES-MIC-64
111: AES-MIC-32

Bit 2-0 **TXNCIPHER[2:0]**: TX Normal FIFO Security Suite Select
000: (default) Undefined
001: AES-ENC
010: AES-ENC-MIC-128
011: AES-ENC-MIC-64
100: AES-ENC-MIC-32
101: AES-MIC-128
110: AES-MIC-64
111: AES-MIC-32

SREG0x2D: SECCR1

SECURITY CONTROL 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	TXBCIPHER2	TXBCIPHER1	TXBCIPHER0	MACTMRFR	r	DISDEC	DISENC
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

Bit 7 **Reserved**: Maintain as '0b0'

Bit 6-4 **TXBCIPHER**: TX Beacon FIFO Security Suite Select
000: (default) Undefined
001: AES-ENC
010: AES-ENC-MIC-128
011: AES-ENC-MIC-64
100: AES-ENC-MIC-32
101: AES-MIC-128
110: AES-MIC-64
111: AES-MIC-32

Bit 3 **MACTMRFR**: MAC Timer Free Run
0: (default) Disable
1: Enable. The free-run value of MAC timer will be attached to every received packet behind RSSI.

Bit 2 **Reserved**: Maintain as '0b0'

Bit 1 **DISDEC**: Disable Decryption Function
0: (default) Enable decryption process
1: Disable the decryption process. The UZ2400 does not generate a security interrupt, even if 'security' bit in the MAC header is detected.

Bit 0 **DISENC**: Disable Encryption Function
0: (default) Enable encryption function
1: Disable the encryption process. The UZ2400 does not encrypt the data, even if the TX security is enabled.

SREG0x2E: TXPEMISP

TRANSMIT PARAMETER							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXPET3	TXPET2	TXPET1	TXPET0	MISP3	MISP2	MISP1	MISP0
R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1

Bit 7-4 **TXPET[3:0]**: VCO Settling Time
0111: (default)
1001: (optimized - Do Not Change)

Bit 3-0 **MISP[3:0]**: Minimum Short Interframe Spacing
0101: (default - Do Not Change)

SREG0x30: RXSR

RX MAC STATUS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RXFFFULL	WRFF1	UPSECERR	RXFFOVFL	RXCRCERR	SECDECERR	r	r
R-0	R-0	R/W1C-0	R-0	R-0	R-0	R-0	R-0

Bit 7 **RXFFFULL**: RX FIFO Full
0: (default) RX FIFO available for data receiving
1: RX FIFO not available for data receiving

Bit 6 **WRFF1**: RX FIFO Status
0: (default) Packet is ready in RX FIFO 0
1: Packet is ready in RX FIFO 1

Bit 5 **UPSECERR**: MIC Error in Upper Layer Security Mode
0: (default) MIC error did not occur
1: MIC error occurred. Write '1' to clear.

Bit 4 **RXFFOVFL**: RX FIFO Overflow
0: (default) Not overflow
1: Overflow

Bit 3 **RXCRCERR**: RX CRC Error
0: (default) RX CRC correct
1: RX CRC error

Bit 2 **SECDECERR**: Security Decryption Error
0: (default) Security decryption correct
1: Security decryption error

Bit 1-0 **Reserved**: Maintain as '0b00'

SREG0x31: ISRSTS

INTERRUPT STATUS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPIF	WAKEIF	MACTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF
RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0

Bit 7 **SLPIF**: Sleep Alert Interrupt (1)
0: (default) No Sleep alert interrupt occurred
1: A sleep alert interrupt occurred

Bit 6 **WAKEIF**: Wake-up Alert Interrupt (1)
0: (default) No wake-up alert interrupt occurred
1: A wake-up interrupt occurred

Bit 5 **MACTMRIF**: MAC timer Interrupt (1)
0: (default) No MAC timer interrupt occurred
1: A MAC timer interrupt occurred

Bit 4 **SECIF**: Security Key Request Interrupt (1)
0: (default) No security key request interrupt occurred
1: A security key request interrupt occurred

Bit 3 **RXIF**: RX FIFO Reception Interrupt (1)
0: (default) No RX FIFO reception interrupt occurred
1: An RX FIFO reception interrupt occurred

Bit 2 **TXG2IF**: TX GTS2 FIFO Transmission Interrupt (1)
0: (default) No TX GTS2 FIFO transmission interrupt occurred
1: A TX GTS2 FIFO transmission interrupt occurred

Bit 1 **TXG1IF**: TX GTS1 FIFO Transmission Interrupt (1)
0: (default) No TX GTS1 FIFO transmission interrupt occurred
1: A TX GTS1 FIFO transmission interrupt occurred

Bit 0 **TXNIF**: TX Normal FIFO Transmission Interrupt (1)
0: (default) No TX Normal FIFO transmission interrupt occurred
1: TX Normal FIFO transmission interrupt occurred

Note 1: Interrupt bits are cleared to '0b0' when the INTSTAT register is read.

SREG0x32: INTMSK

INTERRUPT MASK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPMSK	WAKEMSK	MACTMRMSK	SECMSK	RXMSK	TXG2MSK	TXG1MSK	TXNMSK
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 7 **SLPMSK**: Sleep Alert Interrupt Mask
0: Enable the Sleep alert interrupt
1: (default) Disable the Sleep alert interrupt

Bit 6 **WAKEMSK**: Wake-up Alert Interrupt Mask
0: Enable the wake-up alert interrupt
1: (default) Disable the wake-up alert interrupt

Bit 5 **MACTMRMSK**: MAC Timer Interrupt Mask
0: Enable the MAC timer interrupt
1: (default) Disable the MAC timer interrupt

Bit 4 **SECMSK**: Security Key Request Interrupt Mask
0: Enable security key request interrupt
1: (default) Disable the security key request interrupt

Bit 3 **RXMSK**: RX FIFO Reception Interrupt Mask
0: Enable the RX FIFO reception interrupt
1: (default) Disable the RX FIFO reception interrupt

Bit 2 **TXG2MSK**: TX GTS2 FIFO Transmission Interrupt Mask
0: Enable the TX GTS2 FIFO transmission interrupt
1: (default) Disable the TX GTS2 FIFO transmission interrupt

Bit 1 **TXG1MSK**: TX GTS1 FIFO Transmission Interrupt Mask
0: Enable the TX GTS1 FIFO transmission interrupt
1: (default) Disable the TX GTS1 FIFO transmission interrupt

Bit 0 **TXNMSK**: TX Normal FIFO Transmission Interrupt Mask
0: Enable the TX Normal FIFO transmission interrupt
1: (default) Disable the TX Normal FIFO transmission interrupt

SREG0x33: LRXSR

LAST RX STATUS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	LRXCRCERR	r	r	r
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-4 **Reserved**: Maintain as '0b0000'

Bit 3 **LRXCRCERR**: RX CRC Error Flag

0: (default) RX FIFO CRC correct of the last frame

1: RX FIFO CRC error of the last frame

Bit 2-0 **Reserved**: Maintain as '0b000'

SREG0x34: SPIRXF

SPI AND RX FIFO CONTORL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	BATIND	r	r	r	RDFF1	RXFIFO2
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R/W-0

Bit 7-6 **Reserved**: Maintain as '0b00'

Bit 5 **BATIND**: Battery Low Indicator

0: (default) Battery voltage higher than threshold voltage (1)

1: Battery voltage lower than threshold voltage

Bit 4-2 **Reserved**: Maintain as '0b000'

Bit 1 **RDFF1**: RX FIFO Select to Read

0: (default) Read data from RX FIFO 0

1: Read data from RX FIFO 1

Bit 0 **RXFIFO2**: RX Ping-pong FIFO Enable

0: (default) Disable

1: Enable

Note 1: Threshold voltage is set by LREG0x205[7:4]

SREG0x35: SLPACK

SLEEP ACKNOWLEDGEMENT AND WAKE-UP COUNTER							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPACK	WAKECNT6	WAKECNT5	WAKECNT4	WAKECNT3	WAKECNT2	WAKECNT1	WAKECNT0
WT-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 **SLPACK**: Sleep Acknowledgement

Place the UZ2400 to Power Saving Mode. Bit is automatically cleared to '0' by hardware.

Bit 6-0 **WAKECNT[6:0]**: System Clock Recovery Time

WAKECNT is a 9-bit value. The WAKECNT[8:7] bits are located in SREG0x36[4:3].

0000000: (default)

SREG0x36: RFCTL

RF MODE CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	WAKECNT8	WAKECNT7	RFRST	RFTXMODE	RFRXMODE
R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-5 **Reserved**: Maintain as '0b000'

Bit 4-3 **WAKECNT[8:7]**: System Clock Recovery Time

WAKECNT is a 9-bit value. The WAKECNT [6:0] bits are located in SREG0x35[6:0].

00: (default)

Bit 2 **RFRST**: RF State Machine Reset (1)

0: (default) Normal operation of RF state machine

1: Hold RF state machine in Reset

Bit 1 **RFTXMODE**: Force TX Mode

0: (default) Normal operation of TX mode

1: RF state machine is forced to TX mode

Bit 0 **RFRXMODE**: Force RX Mode

0: (default) Normal operation of RX mode

1: RF state machine is forced to RX mode

Note 1: Perform RF reset by setting RFRST = 1 and then RFRST = 0. Delay at least 192 us after performing to allow RF circuitry to calibrate.

SREG0x37: SECCR2

SECURITY CONTROL 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPDEC	UPENC	TXG2CIPHER2	TXG2CIPHER1	TXG2CIPHER0	TXG1CIPHER2	TXG1CIPHER1	TXG1CIPHER0
WT-0	WT-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 **UPDEC**: Upper Layer Security Decryption Mode
1: Perform upper layer decryption using TX Normal FIFO. Bit is automatically cleared to '0' by hardware.

Bit 6 **UPENC**: Upper Layer Security Encryption Mode
1: Perform upper layer encryption using TX Normal FIFO. Bit is automatically cleared to '0' by hardware.

Bit 5-3 **TXG2CIPHER[2:0]**: TX GTS2 FIFO Security Suite Select
000: (default) Undefined
001: AES-ENC
010: AES-ENC-MIC-128
011: AES-ENC-MIC-64
100: AES-ENC-MIC-32
101: AES-MIC-128
110: AES-MIC-64
111: AES-MIC-32

Bit 2-0 **TXG1CIPHER[2:0]**: TX GTS1 FIFO Security Suite Select
000: (default) Undefined
001: AES-ENC
010: AES-ENC-MIC-128
011: AES-ENC-MIC-64
100: AES-ENC-MIC-32
101: AES-MIC-128
110: AES-MIC-64
111: AES-MIC-32

SREG0x38 BBREG0

BASEBAND REGISTER 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PRECNT3	PRECNT2	PRECNT1	PRECNT0	r	CONT_TX	TURBO1	TURBO0
R/W-1	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

Bit 7-4 **PRECNT[3:0]**: Preamble Number
1000: (default - Do Not Change)

Bit 3 **Reserved**: Maintain as '0b0'

Bit 2 **CONT_TX**: Continuously TX
0: (default) Normal TX operation
1: Continuously send modulated random data

Bit 1-0 **TURBO[1:0]**: Turbo Mode Select
00: (default) 250 kbps Normal mode
01: 1 Mbps Turbo mode
10: Undefined
11: 2 Mbps Turbo mode

SREG0x3A: BBREG2

BASEBAND REGISTER 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CCAMODE1	CCAMODE0	CCATH3	CCATH2	CCATH1	CCATH0	r	r
R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R-1	R-1

Bit 7-6 **CCAMODE[1:0]**: Clear Channel Assessment (CCA) Mode Select
00: Disable CCA mode
01: (default) Carrier sense (CS) mode, which detects IEEE 802.15.4 signals
10: Energy detection (ED) mode, which detects in-band signals
11: Combination of carrier sense mode and energy detection mode

Bit 5-2 **CCATH[3:0]**: Clear Channel Assessment (CCA) Carrier Sense (CS) Threshold
1111: (default)

Bit 1-0 **Reserved**: Maintain as '0b11'

SREG0x3B: BBREG3

BASEBAND REGISTER 3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PREVALIDTH3	PREVALIDTH2	PREVALIDTH1	PREVALIDTH0	PREDETTH3	PREDETTH2	PREDETTH1	PREDETTH0
R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0

Bit 7-4 **PREVALIDTH[3:0]**: Preamble Search Energy Valid Threshold
0101: (optimized - Do Not Change)
1101: (default)

Bit 3-0 **PREDETTH**: Energy Detection Threshold
0000: (optimized - Do Not Change)
1000: (default)

SREG0x3C: BBREG4

BASEBAND REGISTER 4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CSTH3	CSTH2	CSTH1	PRECNT2	PRECNT1	PRECNT0	TXDACEDGE	RXADCEDGE
R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0

Bit 7-5 **CSTH[2:0]**: Baseband Parameter
100: (default - Do Not Change)

Bit 4-2 **PRECNT[2:0]**: Baseband Parameter
111: (default - Do Not Change)

Bit 1 **TXDACEDGE**: Baseband Parameter
0: (default - Do Not Change)

Bit 0 **RXADCEDGE**: Baseband Parameter
0: (default - Do Not Change)

SREG0x3D: BBREG5

BASEBAND REGISTER 5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PEAKLATE4	PEAKLATE3	PEAKLATE2	PEAKLATE1	PEAKLATE0	PEAKEARLY2	PEAKEARLY1	PEAKEARLY0
R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1

Bit 7-3 **PEAKLATE[4:0]**: Upper boundary of preamble searching time
00000: (optimized - Do Not Change)
01111: (default)

Bit 2-0 **PEAKEARLY[2:0]**: Lower boundary of preamble searching time
011: (default)
111: (optimized - Do Not Change)

SREG0x3E: BBREG6

BASEBAND REGISTER 6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RSSIMODE1	RSSIMODE2	RSSIMAXL	r	r	r	r	RSSIRDY
WT-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-1

Bit 7 **RSSIMODE1**: RSSI Mode 1

1: Firmware-initiate RSSI calculation. Wait until **RSSIRDY**=1. Bit is automatically cleared to '0' by hardware.

Bit 6 **RSSIMODE2**: RSSI Mode 2

0: (default) RSSI calculation is not performed for each received packet

1: (optimized - Do Not Change) Calculate RSSI for each received packet. The RSSI value is stored in RXFIFO.

Bit 5 **RSSIMAXL**: Latch Maximum RSSI Value

0: (default) The maximum RSSI value is not kept in LREG0x210

1: For FW request mode, the maximum RSSI value is kept in LREG0x210[7:0]

Bit 4-1 **Reserved**: Maintain as '0b0000'

Bit 0 **RSSIRDY**: RSSI Ready Signal for **RSSIMODE1** bit

If RSSIMODE1 = 1, then

0: RSSI calculation in progress

1: (default) RSSI calculation has finished and the RSSI value is ready in LREG0x210[7:0]

SREG0x3F BBREG7

BASEBAND REGISTER 7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CCAEDTH7	CCAEDTH6	CCAEDTH5	CCAEDTH4	CCAEDTH3	CCAEDTH2	CCAEDTH1	CCAEDTH0
R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **CCAEDTH[7:0]**: Clear Channel Assessment (CCA) Energy Detection (ED) Threshold
If the in-band signal strength is greater than the threshold, the channel is busy. The 8-bit value can be mapped to a power level according to RSSI.
01100000: (default - Do Not Change)

C.2 Long Registers (LREG0x200~LREG0x27F)

0x200	RFCTRL0	0x210	RSSI	0x220	SLPCTRL	0x230	ASSOEADR_0
0x201	RFCTRL1	0x211	IRQCTRL	0x221	Reserved	0x231	ASSOEADR_1
0x202	RFCTRL2	0x212	SADRCTRL	0x222	WAKETIMEL	0x232	ASSOEADR_2
0x203	RFCTRL3	0x213	SRCADR_0	0x223	WAKETIMEH	0x233	ASSOEADR_3
0x204	RFCTRL4	0x214	SRCADR_1	0x224	REMCNTL	0x234	ASSOEADR_4
0x205	RFCTRL5	0x215	SRCADR_2	0x225	REMCNTH	0x235	ASSOEADR_5
0x206	RFCTRL6	0x216	SRCADR_3	0x226	MAINCNT_0	0x236	ASSOEADR_6
0x207	RFCTRL7	0x217	SRCADR_4	0x227	MAINCNT_1	0x237	ASSOEADR_7
0x208	RFCTRL8	0x218	SRCADR_5	0x228	MAINCNT_2	0x238	ASSOSADRL
0x209	SLPCAL_0	0x219	SRCADR_6	0x229	MAINCNT_3	0x239	ASSOSADRH
0x20A	SLPCAL_1	0x21A	SRCADR_7	0x22A	Reserved	0x23A	Reserved
0x20B	SLPCAL_2	0x21B	Reserved	0x22B	Reserved	0x23B	Reserved
0x20C	Reserved	0x21C	Reserved	0x22C	Reserved	0x23C	RXFRMTYPE
0x20D	Reserved	0x21D	Reserved	0x22D	Reserved	0x23D	GPIODIR
0x20E	Reserved	0x21E	HLEN	0x22E	Reserved	0x23E	GPIO
0x20F	Reserved	0x21F	Reserved	0x22F	TESTMODE	0x23F	Reserved

0x240	UPNONCE_0	0x250	RFCTRL50	0x260	Reserved	0x270	Reserved
0x241	UPNONCE_1	0x251	RFCTRL51	0x261	Reserved	0x271	Reserved
0x242	UPNONCE_2	0x252	RFCTRL52	0x262	Reserved	0x272	Reserved
0x243	UPNONCE_3	0x253	RFCTRL53	0x263	Reserved	0x273	RFCTRL73
0x244	UPNONCE_4	0x254	RFCTRL54	0x264	Reserved	0x274	RFCTRL74
0x245	UPNONCE_5	0x255	RFCTRL55	0x265	Reserved	0x275	RFCTRL75
0x246	UPNONCE_6	0x256	Reserved	0x266	Reserved	0x276	RFCTRL76
0x247	UPNONCE_7	0x257	Reserved	0x267	Reserved	0x277	RFCTRL77
0x248	UPNONCE_8	0x258	Reserved	0x268	Reserved	0x278	Reserved
0x249	UPNONCE_9	0x259	RFCTRL59	0x269	Reserved	0x279	Reserved
0x24A	UPNONCE_10	0x25A	Reserved	0x26A	Reserved	0x27A	INITCNTL
0x24B	UPNONCE_11	0x25B	Reserved	0x26B	Reserved	0x27B	INITCNTH
0x24C	UPNONCE_12	0x25C	Reserved	0x26C	Reserved	0x27C	Reserved
0x24D	SECCTRL	0x25D	Reserved	0x26D	Reserved	0x27D	Reserved
0x24E	ENCFLG	0x25E	Reserved	0x26E	Reserved	0x27E	Reserved
0x24F	AUTFLG	0x25F	Reserved	0x26F	Reserved	0x27F	Reserved

LREG0x200: RFCTRL0

RF CONTROL 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CHANNEL3	CHANNEL2	CHANNEL1	CHANNEL0	r	r	PSCTRL1	PSCTRL0
R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-1

Bit 7-4 **CHANNEL[3:0]**: Channel Number
IEEE 802.15.4 2.4GHz band channels (11~26)
0000: Channel 11, 2405 MHz (default)
0001: Channel 12, 2410 MHz
0010: Channel 13, 2415 MHz
0011: Channel 14, 2420 MHz
0100: Channel 15, 2425 MHz
0101: Channel 16, 2430 MHz
0110: Channel 17, 2435 MHz
0111: Channel 18, 2440 MHz
1000: Channel 19, 2445 MHz
1001: Channel 20, 2450 MHz
1010: Channel 21, 2455 MHz
1011: Channel 22, 2460 MHz
1100: Channel 23, 2465 MHz
1101: Channel 24, 2470 MHz
1110: Channel 25, 2475 MHz
1111: Channel 26, 2480 MHz

Bit 3-2 **Reserved**: Maintain as '0b00'

Bit 1-0 **PSCTRL**: Prescalar Control
01: (default)
11: (optimized - Do Not Change)

LREG0x201: RFCTRL1

RF CONTROL 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	r	VCORX1	VCORX0
R-0	R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-1

Bit 7-2 **Reserved**: Maintain as '0b000000'

Bit 1-0 **RXVCO[1:0]**: RX VCO

01: (default)

10: (optimized - Do Not Change)

LREG0x202: RFCTRL2

RF CONTROL 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PLLDMY	RXFC0-1	RXFC0-0	r	r	RSSIBA2	RSSIBA1	RSSIBA0
R-1	R/W-0	R/W-0	R-0	R-0	R/W-1	R/W-0	R/W-0

Bit 7 **PLLDMY**: Dummy Pre-Scalar Load
0: (optimized - Do Not Change)
1: (default)

Bit 6-5 **RXFC0[1:0]**: RX Filter Control 0
00: (default)
11: (optimized - Do Not Change)

Bit 4-3 **Reserved**: Maintain as '0b00'

Bit 2-0 **RSSIBA[2:0]**: RSSI Base Adjustment
100: (default)
110: (optimized - Do Not Change) for IEEE 802.15.4™ defined range

LREG0x203: RFCTRL3

RF CONTROL 3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXGB4	TXGB3	TXGB2	TXGB1	TXGB0	r	r	r
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0

Bit 7-3 **TXGB[4:0]**: TX Gain Control in dB (1)

Gain step is monotonic and nonlinear. Resolution is variable between chips.

00000: 0 dBm (default)	10000: -3.1 dBm
00001: -0.1 dBm	10001: -3.3 dBm
00010: -0.3 dBm	10010: -3.6 dBm
00011: -0.6 dBm	10011: -3.8 dBm
00100: -0.9 dBm	10100: -4.2 dBm
00101: -1.1 dBm	10101: -4.4 dBm
00110: -1.2 dBm	10110: -4.7 dBm
00111: -1.3 dBm	10111: -5.0 dBm
01000: -1.4 dBm	11000: -5.3 dBm
01001: -1.5 dBm	11001: -5.7 dBm
01010: -1.7 dBm	11010: -6.2 dBm
01011: -2.0 dBm	11011: -6.5 dBm
01100: -2.2 dBm	11100: -6.9 dBm
01101: -2.4 dBm	11101: -7.4 dBm
01110: -2.6 dBm	11110: -7.9 dBm
01111: -2.8 dBm	11111: -8.3 dBm

Bit 2-0 **Reserved**: Maintain as '0b000'

Note1: Please refer to Appendix B for detail.

LREG0x204: RFCTRL4

RF CONTROL 4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RXFBW4	RXFBW3	RXFBW2	RXFBW1	RXFBW0	RXFCO	RXD2O1	RXD2O0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-3 **RXFC1[4:0]**: RX Filter Control 1
00000: (default - Do Not Change)

Bit 2 **RXFCO**: RX Filter Calibration Output
0: (default)
1: (optimized - Do Not Change)

Bit 1-0 **RXD2O[1:0]**: RX Divide-by-2 Option
00: (default)
10: (optimized - Do Not Change)

LREG0x205: RFCTRL5

RF CONTROL 5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
BATTH3	BATTH2	BATTH1	BATTH0	r	r	r	r
R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0

Bit 7-4 **BATTH**: Battery Monitor Threshold
0000: 1.8 V (default)
0001: 1.9 V
0010: 2.0 V
0011: 2.1 V
0100: 2.2 V
0101: 2.3 V
0110: 2.4 V
0111: 2.5 V
1000: 2.6 V
1001: 2.7 V
1010: 2.8 V
1011: 2.9 V
1100: 3.0 V
1101: 3.3 V
1110: 3.4 V
1111: 3.6 V

Bit 3-0 **Reserved**: Maintain as '0b0000'

LREG0x206: RFCTRL6

RF CONTROL 6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXFBW1	TXFBW0	32MXCO1	32MCCO0	BATEN	r	r	r
R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R-0	R-0	R-0

Bit 7-6 **TXFBW[1:0]**: TX Filter
00: Optimized for 250 kbps normal mode
01: Optimized for 1M/2M bps turbo mode

Bit 5-4 **32MXCO[1:0]**: 32MHz Crystal Oscillator
01: (optimized - Do Not Change)

Bit 3 **BATEN**: Battery Monitor Enable
0: Disable (default)
1: Enable

Bit 2-0 **Reserved**: Maintain as '0b000'

LREG0x207: RFCTRL7

RF CONTROL 7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
OUTCLK2	OUTCLK1	OUTCLK0	RXFC2	TXFS1	TXFS0	r	r
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

Bit 7-5 **OUTCLK**: Output Clock Frequency Option [1]
- 000: 1 MHz (default)
- 001: 2 MHz
- 010: 4 MHz
- 011: 8 MHz
- 100: 16 MHz
- 101: 32 MHz
- 110: Undefined
- 111: Disable clock output

Bit 4 **RXFC2**: RX Filter Control 2
- 0: (default) For 250k bps normal mode and 2M bps turbo mode
- 1: For 1M bps turbo mode

Bit 3-2 **TXFS**: Center frequency of TX matching circuit compensation
- 00: (default) Optimized for 1M/2M bps turbo mode
- 11: Optimized for 250 kbps normal mode

Bit 1-0 **Reserved**: Maintain as '0b00'

Note 1: It is recommended to set LREG0x277=0x04 if clock output is enabled.

LREG0x208: RFCTRL8

RF CONTROL 8							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXD2CO1	TXD2CO0	r	r	r	r	r	r
R/W-0	R/W-0	R-0	R-0	R-1	R-1	R-0	R-0

Bit 7-6 **TXD2O[1:0]**: TX Divide-by-2 Option
00: (default)
10: (optimized - Do Not Change)

Bit 5-0 **Reserved**: Maintain as '0b001100'

LREG0x209: SLPCAL_0

SLEEP CLOCK CALIBRATION 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPCAL7	SLPCAL6	SLPCAL5	SLPCAL4	SLPCAL3	SLPCAL2	SLPCAL1	SLPCAL0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SLPCAL[7:0]**: Sleep Clock Calibration Counter
A 20-bit calibration counter which calibrates the sleep clock. SLPCAL[19:0] indicates the time period of 16 sleep clock cycles. The unit is 62.5ns, counted by the 16 MHz.

LREG0x20A: SLPCAL_1

SLEEP CLOCK CALIBRATION 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPCAL15	SLPCAL14	SLPCAL13	SLPCAL12	SLPCAL11	SLPCAL10	SLPCAL9	SLPCAL8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SLPCAL[15:8]**: Sleep Clock Calibration Counter
A 20-bit calibration counter which calibrates the sleep clock. SLPCAL[19:0] indicates the time period of 16 sleep clock cycles. The unit is 62.5ns, counted by the 16 MHz.

LREG0x20B: SLPCAL_2

SLEEP CLOCK CALIBRATION 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPCALRDY	r	r	SLPCALEN	SLPCAL19	SLPCAL18	SLPCAL17	SLPCAL16
R-0	R-0	R-0	WT-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 **SLPCALRDY**: Sleep Clock Calibration Ready
0: (default) Not Ready
1: Sleep clock calibration counter is ready to be read.

Bit 6-5 **Reserved**: Maintain as '0b00'

Bit 4 **SLPCALEN**: Sleep Clock Calibration Enable
1: Starts the sleep clock calibration counter. Bit is automatically cleared to '0' by hardware.

Bit 3-0 **SLPCAL[19:16]**: Sleep Clock Calibration Counter
A 20-bit calibration counter which calibrates the sleep clock. SLPCAL[19:0] indicates the time period of 16 sleep clock cycles. The unit is 62.5ns, counted by the 16 MHz.

LREG0x210: RSSI

RSSI							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RSSI7	RSSI6	RSSI5	RSSI4	RSSI3	RSSI2	RSSI1	RSSI0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-0 **RSSI[7:0]**: RSSI value

If SREG0x3E[0]=1, the RSSI register contains the average RSSI received power level for 128 us.

00000000: (default)

LREG0x211: IRQCTRL

INTERRUPT CONTROL 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	r	IRQPOL	r
R-0	R-0	R-0	R-0	R-0	R-0	R/W-0	R-0

Bit 7-2 **Reserved**: Maintain as '0b000000'

Bit 1 **IRQPOL**: Interrupt Edge Polarity

0: (default) Falling edge

1: Rising edge

Bit 0 **Reserved**: Maintain as '0b0'

LREG0x212: SADRCTRL

SOURCE ADDRESS CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	r	SADRMODE1	SADRMODE0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-2 **Reserved**: Maintain as '0b000000'

Bit 1-0 **SADRMODE[1:0]**: Source Address Mode

00: Reserved (default)

01: Reserved

10: 16-bit short address

11: 64-bit extended address

LREG0x213: SRCADR_0

SOURCE ADDRESS 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SRCADR7	SRCADR6	SRCADR5	SRCADR4	SRCADR3	SRCADR2	SRCADR1	SRCADR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SRCADR[7-0]**: Received Packet Source Address

LREG0x214: SRCADR_1

SOURCE ADDRESS 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SRCADR15	SRCADR14	SRCADR13	SRCADR12	SRCADR11	SRCADR10	SRCADR9	SRCADR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SRCADR[15-8]**: Received Packet Source Address

LREG0x215: SRCADR_2

SOURCE ADDRESS 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SRCADR23	SRCADR22	SRCADR21	SRCADR20	SRCADR19	SRCADR18	SRCADR17	SRCADR16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SRCADR[23-16]**: Received Packet Source Address

LREG0x216: SRCADR_3

SOURCE ADDRESS 3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SRCADR31	SRCADR30	SRCADR29	SRCADR28	SRCADR27	SRCADR26	SRCADR25	SRCADR24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SRCADR[31-24]**: Received Packet Source Address

LREG0x217: SRCADR_4

SOURCE ADDRESS 4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SRCADR39	SRCADR38	SRCADR37	SRCADR36	SRCADR35	SRCADR34	SRCADR33	SRCADR32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SRCADR[39-32]**: Received Packet Source Address

LREG0x218: SRCADR_5

SOURCE ADDRESS 5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SRCADR47	SRCADR46	SRCADR45	SRCADR44	SRCADR43	SRCADR42	SRCADR41	SRCADR40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SRCADR[47-40]**: Received Packet Source Address

LREG0x219: SRCADR_6

SOURCE ADDRESS 6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SRCADR55	SRCADR54	SRCADR53	SRCADR52	SRCADR51	SRCADR50	SRCADR49	SRCADR48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SRCADR[55-48]**: Received Packet Source Address

LREG0x21A: SRCADR_7

SOURCE ADDRESS 7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SRCADR63	SRCADR62	SRCADR61	SRCADR60	SRCADR59	SRCADR58	SRCADR57	SRCADR56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **SRCADR[63-56]**: Received Packet Source Address

LREG0x21E: HLEN

HEADER LENGTH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	HLEN5	HLEN4	HLEN3	HLEN2	HLEN1	HLEN0
R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-6 **Reserved**: Maintain as '0b00'

Bit 5-0 **HLEN[5:0]**: Header Length for Decryption Process in RX FIFO

Header length of the received packet including frame control field, sequence number and address information. If a user-defined header length (including auxiliary header length) is used, user shall update the length value by writing **HLEN[5:0]** back after security interrupt received.

000000: (default)

LREG0x220: SLPCTRL

SLEEP CLOCK CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	SCLKDIV4	SCLKDIV3	SCLKDIV2	SCLKDIV1	SCLKDIV0
R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-5 **Reserved**: Maintain as '0b000'

Bit 4-0 **SCLKDIV[4:0]**: Sleep Clock Divisor

Sleep clock is divided by $2^{SLPCLKDIV}$.

00000: 0 (default)

…

11111: 31

LREG0x222: WAKETIMEL

WAKE-UP TIME MATCH VALUE LOW BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
WAKETIME7	WAKETIME6	WAKETIME5	WAKETIME4	WAKETIME3	WAKETIME2	WAKETIME1	WAKETIME0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0

Bit 7 **WAKETIME[7:0]**: Wake Time Match Value, Low Byte

LREG0x223: WAKETIMEH

WAKE-UP TIME MATCH VALUE HIGH BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	WAKETIME10	WAKETIME9	WAKETIME8
R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0

Bit 7 **WAKETIME[10:8]**: Wake Time Match Value, High Byte

WAKETIME is an 11-bit value. In sleep mode, when the Main Counter is down counting to the value of WAKETIME, the 32 MHz main oscillator will start to be recovered. Note that the value of WAKETIME has to be greater than that of WAKECNT.

000 00000000: Undefined
000 00000001: 1 sleep clock
…
000 00001010: (default) 10 sleep clocks
…
111 11111111: 2047 sleep clocks

LREG0x224: REMCNTL

REMAIN COUNTER LOW BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
REMCNT7	REMCNT6	REMCNT5	REMCNT4	REMCNT3	REMCNT2	REMCNT1	REMCNT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **REMCNT[7:0]**: Remain Counter, Low Byte

LREG0x225: REMCNTH

REMAIN COUNTER HIGH BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
REMCNT15	REMCNT14	REMCNT13	REMCNT12	REMCNT11	REMCNT10	REMCNT9	REMCNT8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **REMCNT[15:8]**: Remain Counter, High Byte

Remain counter is a 16-bit counter. Unit: 62.5 ns

LREG0x226: MAINCNT_0

MAIN COUNTER 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
MAINCNT7	MAINCNT6	MAINCNT5	MAINCNT4	MAINCNT3	MAINCNT2	MAINCNT1	MAINCNT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **MAINCNT[7:0]**: Main Counter
Main counter (1) is a 26-bit counter. Units: Sleep Clock Period (2)

LREG0x227: MAINCNT_1

MAIN COUNTER 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
MAINCNT15	MAINCNT14	MAINCNT13	MAINCNT12	MAINCNT11	MAINCNT10	MAINCNT9	MAINCNT8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **MAINCNT[15:8]**: Main Counter

LREG0x228: MAINCNT_2

MAIN COUNTER 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
MAINCNT23	MAINCNT22	MAINCNT21	MAINCNT20	MAINCNT19	MAINCNT18	MAINCNT17	MAINCNT16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **MAINCNT[23:16]**: Main Counter

LREG0x229: MAINCNT_3

MAIN COUNTER 3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
STARTCNT	r	r	r	r	r	MAINCNT25	MAINCNT24
WT-0	R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0

Bit 7 **STARTCNT**: Start Sleep Counters
1 = Trigger sleep for Non-beacon mode (BO = 0b1111 and Slotted = 0b0). Bit is automatically cleared to '0' by hardware.
Bit 6-2 **Reserved**: Maintain as '0b00000'
Bit 1-0 **MAINCNT[25:24]**: Main Counter

Note 1: Refer to Section 3.4.6 "Counters for Power Saving Modes" for detail
2: Refer to Section 4.2.5 "Clock Recovery Time" for detail

LREG0x22F TESTMODE

TEST MODE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
MSPI	RSSIRDY1	RSSIRDY0	RSSIWAIT1	RSSIWAIT0	TESTMODE2	TESTMODE1	TESTMODE0
R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0

Bit 7 **MSPI**: Multiple SPI Operation
0: (default) Single SPI operation, SO will be Low when SPI inactive
1: Enable multiple SPI operation, SO will be High-Z state when SPI inactive

Bit 6-5 **RSSIRDY[1:0]**: RSSI wait time for RSSI ready time
01: (optimized - Do Not Change)

Bit 4-3 **RSSIWAIT[1:0]**: RSSI state machine parameter.
01: (optimized - Do Not Change)

Bit 2-0 **TESTMODE**: Special Operation
000: (default) Normal operation
001: GPIO0, GPIO1 and GPIO2 are configured to control external PA, LNA and switch
101: Single-Tone test mode
Others: Undefined

LREG0x230: ASSOEADR_0

ASSOCIATED COORDINATOR EXTENDED ADDRESS 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR7	ASSOEADR6	ASSOEADR5	ASSOEADR4	ASSOEADR3	ASSOEADR2	ASSOEADR1	ASSOEADR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ASSOEADR[7:0]**: 64-Bit Extended Address of Associated Coordinator

LREG0x231: ASSOEADR_1

ASSOCIATED COORDINATOR EXTENDED ADDRESS 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR15	ASSOEADR14	ASSOEADR13	ASSOEADR12	ASSOEADR11	ASSOEADR10	ASSOEADR9	ASSOEADR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ASSOEADR[15:8]**: 64-Bit Extended Address of Associated Coordinator

LREG0x232: ASSOEADR_2

ASSOCIATED COORDINATOR EXTENDED ADDRESS 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR23	ASSOEADR22	ASSOEADR21	ASSOEADR20	ASSOEADR19	ASSOEADR18	ASSOEADR17	ASSOEADR16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ASSOEADR[23:16]**: 64-Bit Extended Address of Associated Coordinator

LREG0x233: ASSOEADR_3

ASSOCIATED COORDINATOR EXTENDED ADDRESS 3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR31	ASSOEADR30	ASSOEADR29	ASSOEADR28	ASSOEADR27	ASSOEADR26	ASSOEADR25	ASSOEADR24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ASSOEADR[31:24]**: 64-Bit Extended Address of Associated Coordinator

LREG0x234: ASSOEADR_4

ASSOCIATED COORDINATOR EXTENDED ADDRESS 4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR39	ASSOEADR38	ASSOEADR37	ASSOEADR36	ASSOEADR35	ASSOEADR34	ASSOEADR33	ASSOEADR32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ASSOEADR[39:32]**: 64-Bit Extended Address of Associated Coordinator

LREG0x235: ASSOEADR_5

ASSOCIATED COORDINATOR EXTENDED ADDRESS 5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR47	ASSOEADR46	ASSOEADR45	ASSOEADR44	ASSOEADR43	ASSOEADR42	ASSOEADR41	ASSOEADR40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ASSOEADR[47:40]**: 64-Bit Extended Address of Associated Coordinator

LREG0x236: ASSOEADR_6

ASSOCIATED COORDINATOR EXTENDED ADDRESS 6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR55	ASSOEADR54	ASSOEADR53	ASSOEADR52	ASSOEADR51	ASSOEADR50	ASSOEADR49	ASSOEADR48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ASSOEADR[55:48]**: 64-Bit Extended Address of Associated Coordinator

LREG0x237: ASSOEADR_7

ASSOCIATED COORDINATOR EXTENDED ADDRESS 7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR63	ASSOEADR62	ASSOEADR61	ASSOEADR60	ASSOEADR59	ASSOEADR58	ASSOEADR57	ASSOEADR56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ASSOEADR[63:56]**: 64-Bit Extended Address of Associated Coordinator

LREG0x238: ASSOSADRL

ASSOCIATED COORDINATOR SHORT ADDRESS LOW BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOSADR7	ASSOSADR6	ASSOSADR5	ASSOSADR4	ASSOSADR3	ASSOSADR2	ASSOSADR1	ASSOSADR0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ASSOSADR[7:0]**: 16-Bit Short Address of Associated Coordinator, Low Byte

LREG0x239: ASSOSADRH

ASSOCIATED COORDINATOR SHORT ADDRESS HIGH BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOSADR15	ASSOSADR14	ASSOSADR13	ASSOSADR12	ASSOSADR11	ASSOSADR10	ASSOSADR9	ASSOSADR8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ASSOSADR[15:8]**: 16-Bit Short Address of Associated Coordinator, High Byte

LREG0x23C: RXFRMTYPE

RX FIFO PACKET FILTER							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RXFTYPE7	RXFTYPE6	RXFTYPE5	RXFTYPE4	RXFTYPE3	RXFTYPE2	RXFTYPE1	RXFTYPE0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1

Bit 7-0 **RXFTYPE[7:0]**: RX Frame Type Filter
00001011: (default - Do Not Change)

LREG0x23D: GPIODIR

GPIO PIN DIRECTION							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	GPIO3DIR	GPIO2DIR	GPIO1DIR	GPIO0DIR
R-0	R-0	R-1	R-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 7-4 **Reserved**: Maintain as '0b0000'

Bit 3 **GPIO3DIR**: General Purpose I/O GPIO3 Direction
0: Output
1: (default) Input

Bit 2 **GPIO2DIR**: General Purpose I/O GPIO2 Direction
0: Output
1: (default) Input

Bit 1 **GPIO1DIR**: General Purpose I/O GPIO1 Direction
0: Output
1: (default) Input

Bit 0 **GPIO0DIR**: General Purpose I/O GPIO0 Direction
0: Output
1: (default) Input

LREG0x23E: GPIO

GPIO PIN							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	GPIO3	GPIO2	GPIO1	GPIO0
R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-4 **Reserved**: Maintain as '0b0000'

Bit 3 **GPIO3**: Setting for output / Status for input of General Purpose I/O Pin GPIO3
0: (default)

Bit 2 **GPIO2**: Setting for output / Status for input of General Purpose I/O Pin GPIO2
0: (default)

Bit 1 **GPIO1**: Setting for output / Status for input of General Purpose I/O Pin GPIO1
0: (default)

Bit 0 **GPIO0**: Setting for output / Status for input of General Purpose I/O Pin GPIO0
0: (default)

LREG0x240: UPNONCE_0

UPPER NONCE SECURITY 0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE7	UPNONCE6	UPNONCE5	UPNONCE4	UPNONCE3	UPNONCE2	UPNONCE1	UPNONCE0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[7:0]**: 104-Bit Upper NONCE Value

LREG0x241: UPNONCE_1

UPPER NONCE SECURITY 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE15	UPNONCE14	UPNONCE13	UPNONCE12	UPNONCE11	UPNONCE10	UPNONCE9	UPNONCE8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[15:8]**: 104-Bit Upper NONCE Value

LREG0x242: UPNONCE_2

UPPER NONCE SECURITY 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE23	UPNONCE22	UPNONCE21	UPNONCE20	UPNONCE19	UPNONCE18	UPNONCE17	UPNONCE16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[23:16]**: 104-Bit Upper NONCE Value

LREG0x243: UPNONCE_3

UPPER NONCE SECURITY 3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE31	UPNONCE30	UPNONCE29	UPNONCE28	UPNONCE27	UPNONCE26	UPNONCE25	UPNONCE24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[31:24]**: 104-Bit Upper NONCE Value

LREG0x244: UPNONCE_4

UPPER NONCE SECURITY 4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE39	UPNONCE38	UPNONCE37	UPNONCE36	UPNONCE35	UPNONCE34	UPNONCE33	UPNONCE32
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[39:32]**: 104-Bit Upper NONCE Value

LREG0x245: UPNONCE_5

UPPER NONCE SECURITY 5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE47	UPNONCE46	UPNONCE45	UPNONCE44	UPNONCE43	UPNONCE42	UPNONCE41	UPNONCE40
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[47:40]**: 104-Bit Upper NONCE Value

LREG0x246: UPNONCE_6

UPPER NONCE SECURITY 6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE55	UPNONCE54	UPNONCE53	UPNONCE52	UPNONCE51	UPNONCE50	UPNONCE49	UPNONCE48
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[55:48]**: 104-Bit Upper NONCE Value

LREG0x247: UPNONCE_7

UPPER NONCE SECURITY 7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE63	UPNONCE62	UPNONCE61	UPNONCE60	UPNONCE59	UPNONCE58	UPNONCE57	UPNONCE56
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[63:56]**: 104-Bit Upper NONCE Value

LREG0x248: UPNONCE_8

UPPER NONCE SECURITY 8							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE71	UPNONCE70	UPNONCE69	UPNONCE68	UPNONCE67	UPNONCE66	UPNONCE65	UPNONCE64
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[71:64]**: 104-Bit Upper NONCE Value

LREG0x249: UPNONCE_9

UPPER NONCE SECURITY 8							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE79	UPNONCE78	UPNONCE77	UPNONCE76	UPNONCE75	UPNONCE74	UPNONCE73	UPNONCE72
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[79:72]**: 104-Bit Upper NONCE Value

LREG0x24A: UPNONCE_10

UPPER NONCE SECURITY 10							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE87	UPNONCE86	UPNONCE85	UPNONCE84	UPNONCE83	UPNONCE82	UPNONCE81	UPNONCE80
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[87:80]**: 104-Bit Upper NONCE Value

LREG0x24B: UPNONCE_11

UPPER NONCE SECURITY 11							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE95	UPNONCE94	UPNONCE93	UPNONCE92	UPNONCE91	UPNONCE90	UPNONCE89	UPNONCE88
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[95:88]**: 104-Bit Upper NONCE Value

LREG0x24C: UPNONCE_12

UPPER NONCE SECURITY 12							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE103	UPNONCE102	UPNONCE101	UPNONCE100	UPNONCE99	UPNONCE98	UPNONCE97	UPNONCE96
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **UPNONCE[103:96]**: 104-Bit Upper NONCE Value

LREG0x24D: SECCTRL

SECURITY CONTROL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	SEC_2006	USRFLAG	r	r	r	r
R-0	R-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0

Bit 7-6 **Reserved**: Maintain as '0b00'

Bit 5 **SEC_2006**: Enable IEEE802.15.4-2006-compliant Block Cipher Mode
0: (default) Disable
1: Enable

Bit 4 **USRFLAG**: User Defined Flag and initial Counter (1)
0: (default) Disable
1: Enable

Bit 3-0 **Reserved**: Maintain as '0b0000'

Note 1: User-defined flag is defined in LREG0x24E and LREG0x24F. User-defined counter is defined in LREG0x27A and LREG0x27B.

LREG0x24E: ENCFLG

ENCRYPTION							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ENCFLG7	ENCFLG6	ENCFLG5	ENCFLG4	ENCFLG3	ENCFLG2	ENCFLG1	ENCFLG0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **ENCFLG**: Encryption Flag

User-defined flag for encryption in CCM/CCM* mode of Upper Cipher operation. Only works when LREG0x24D[4] = '1'.

00000000: (default)

LREG0x24F: AUTFLG

AUTHENTICATION							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
AUTFLG7	AUTFLG6	AUTFLG5	AUTFLG4	AUTFLG3	AUTFLG2	AUTFLG1	AUTFLG0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **AUTFLG**: Authentication Flag

User-defined flag for authentication in CBC-MAC mode of Upper Cipher operation. Only works when LREG0x24D[4] = '1'.

00000000: (default)

LREG0x250: RFCTRL50

RF CONTROL 50							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	DCPOC	DCOPC3	DCOPC2	DCOPC1	DCOPC0
R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-5 **Reserved**: Maintain as '0b000'

Bit 4 **DCPOC**: DC-DC Converter Power Control

0: Bypass (default)

1: Enable

Bit 3-0 **DCOPC[3:2]**: DC-DC Converter Optimization Control

0000: (default)

0111: (optimized - Do Not Change)

LREG0x251: RFCTRL51

RF CONTROL 51							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
DCOPC5	DCOPC4	r	r	r	r	r	r
R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-6 **DCOPC[5:4]**: DC-DC Converter Optimization Control

00: (default)

11: (optimized - Do Not Change)

Bit 5-0 **Reserved**: Maintain as '0b000000'

LREG0x252: RFCTRL52

RF CONTROL 52							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLCTRL6	SLCTRL5	SLCTRL4	SLCTRL3	SLCTRL2	SLCTRL1	SLCTRL0	32MXCTRL
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 7-1 **SLCTRL**: Sleep Clock Control
0000000: (optimized - Do Not Change)
1111111: (default)

Bit 0 **32MXCTRL**: Start-up Circuit in 32MHz Crystal Oscillator Control
0: Disable
1: Enable (default)

LREG0x253: RFCTRL53

RF CONTROL 53							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	FIFOPS	DIGITALPS	r	PA1CFEN	PA1CTRLF-2	PA1CTRLF-1	PA1CTRLF-0
R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 **Reserved**: Maintain as '0b0'

Bit 6 **FIFOPS**: FIFO Power while Sleep
0: (default) VDD
1: GND

Bit 5 **DIGITALPS**: Digital Power while Sleep (1)
0: (default) VDD
1: GND

Bit 4 **Reserved**: Maintain as '0b0'

Bit 3 **PA1CFEN**: PA 1 Control Fine-tuning Enable
0: (default) Disable
1: Enable

Bit 2-0 **PA1CTRLF[2:0]**: PA 1 Control Fine-tuning (2)
1st stage PA current fine tuning
000: (default)

Note 1: Please be noted that if the bit is set to '1', the value of all the registers are not able to be read back.
Note 2: Please follow the TX output power setting listed in Appendix B.

LREG0x254: RFCTRL54

RF CONTROL 54							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
1MCSEN	1MFRCH6	1MCSCH5	1MCSCH4	1MCSCH3	1MCSCH2	1MCSCH1	1MCSCH0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7 **1MCSEN**: 1 MHz Channel Spacing Enable

0: Disable (default)

1: Enable. When LREG0x254[7]=1, RF channel can only be selected by LREG0x254[6:0] and the setting of LREG0x200[7:4] will not change the channel number at all.

Bit 6-0 **1MCSCH**: 1 MHz Channel Spacing Channel Number

LREG0x254[6:0] only works when LREG254[7]=1.

0000000: 2400 MHz	0100001: 2433 MHz	1000010: 2466 MHz
0000001: 2401 MHz	0100010: 2434 MHz	1000011: 2467 MHz
0000010: 2402 MHz	0100011: 2435 MHz	1000100: 2468 MHz
0000011: 2403 MHz	0100100: 2436 MHz	1000101: 2469 MHz
0000100: 2404 MHz	0100101: 2437 MHz	1000110: 2470 MHz
0000101: 2405 MHz	0100110: 2438 MHz	1000111: 2471 MHz
0000110: 2406 MHz	0100111: 2439 MHz	1001000: 2472 MHz
0000111: 2407 MHz	0101000: 2440 MHz	1001001: 2473 MHz
0001000: 2408 MHz	0101001: 2441 MHz	1001010: 2474 MHz
0001001: 2409 MHz	0101010: 2442 MHz	1001011: 2475 MHz
0001010: 2410 MHz	0101011: 2443 MHz	1001100: 2476 MHz
0001011: 2411 MHz	0101100: 2444 MHz	1001101: 2477 MHz
0001100: 2412 MHz	0101101: 2445 MHz	1001110: 2478 MHz
0001101: 2413 MHz	0101110: 2446 MHz	1001111: 2479 MHz
0001110: 2414 MHz	0101111: 2447 MHz	1010000: 2480 MHz
0001111: 2415 MHz	0110000: 2448 MHz	1010001: 2481 MHz
0010000: 2416 MHz	0110001: 2449 MHz	1010010: 2482 MHz
0010001: 2417 MHz	0110010: 2450 MHz	1010011: 2483 MHz
0010010: 2418 MHz	0110011: 2451 MHz	1010100: 2484 MHz
0010011: 2419 MHz	0110100: 2452 MHz	1010101: 2485 MHz
0010100: 2420 MHz	0110101: 2453 MHz	1010110: 2486 MHz
0010101: 2421 MHz	0110110: 2454 MHz	1010111: 2487 MHz
0010110: 2422 MHz	0110111: 2455 MHz	1011000: 2488 MHz
0010111: 2423 MHz	0111000: 2456 MHz	1011001: 2489 MHz
0011000: 2424 MHz	0111001: 2457 MHz	1011010: 2490 MHz
0011001: 2425 MHz	0111010: 2458 MHz	1011011: 2491 MHz
0011010: 2426 MHz	0111011: 2459 MHz	1011100: 2492 MHz
0011011: 2427 MHz	0111100: 2460 MHz	1011101: 2493 MHz
0011100: 2428 MHz	0111101: 2461 MHz	1011110: 2494 MHz
0011101: 2429 MHz	0111110: 2462 MHz	1011111: 2495 MHz
0011110: 2430 MHz	0111111: 2463 MHz	1100000: Undefined
0011111: 2431 MHz	1000000: 2464 MHz	…
0100000: 2432 MHz	1000001: 2465 MHz	1111111: Undefined

REG0x255: RFCTRL55

RF CONTROL 55							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	HALTCTRL	r	r	r	r	r
R-0	R-0	R/W-0	R-0	R-0	R-0	R-0	R-0

Bit 7-6 **Reserved**: Maintain as '0b00'

Bit 5 **HALTCTRL**: Halt Mode Control (1)

0: Disable (default)

1: Enable

Bit 4-0 **Reserved**: Maintain as '0b00000'

Note 1: Before entering into Halt Mode, LREG0x277 has to be set to 0x04.

LREG0x259 RFCTRL59

RF CONTROL 59							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	r	r	PLLOPT4
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R/W-1

Bit 7-1 **Reserved**: Maintain as '0b0000000'

Bit 0 **PLLOPT[4]**: PLL Performance Optimization

0: (optimized - Do Not Change)

1: (default)

LREG0x273: RFCTRL73

RF CONTROL 73							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
VCOTXOPT1	VCOTXOPT0	r	ADCOPT	PLLOPT3	PLLOPT2	PLLOPT1	PLLOPT0
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-6 **VCOTXOPT[1:0]**: VCO for TX Optimization
00: (default)
10: (optimized - Do Not Change)

Bit 5 **Reserved**: Maintain as '0b0'

Bit 4 **ADCOPT**: ADC Optimization
0: (default)
1: Optimized for 1.8v≦Vdd＜2.0v

Bit 3-0 **PLLOPT[3:0]**: PLL Performance Optimization
0000: (default)
1111: Optimized for 1.8v≦Vdd＜2.0v

LREG0x274: RFCTRL74

RF CONTROL 74							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PA1CCEN	PA1CTRLC-2	PA1CTRLC-1	PA1CTRLC-0	PA2CTRL-3	PA2CTRL-2	PA2CTRL-1	PA2CTRL-0
R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0

Bit 7 **PA1CCEN**: PA 1 Control Coarse-tuning Enable
0: Disable
1: Enable (default)

Bit 6-4 **PA1CTRLC[2:0]**: PA 1 Control Coarse-tuning (1)
1st stage PA current coarse tuning
100: (default)

Bit 3-0 **PA2CTRL[3:0]**: PA 2 Control (1)
2nd stage PA current control
0000: Optimized for 1.8v≦Vdd＜2.0v
0101: Optimized for 2.0v≦Vdd≦3.6v
1010: (default)

Note 1: Please follow the TX output power setting listed in Appendix B.

LREG0x275: RFCTRL75

RF CONTROL 75							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	SCLKSEL	SCLKOPT3	SCLKOPT2	SCLKOPT1	SCLKOPT0
R-0	R-0	R-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1

Bit 7-5 **Reserved**: Maintain as '0b000'

Bit 4 **SCLKSEL**: Sleep Clock Select

0: External 32 KHz Crystal Oscillator

1: (default) Integrated Ring Oscillator

Bit 3-0 **SCLKOPT**: Sleep Clock Optimization

0011: (optimized - Do Not Change)

0101: (default)

LREG0x276: RFCTRL76

RF CONTROL 76							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	r	r	r	SCLKOPT6	SCLKOPT5	SCLKOPT4
R-0	R-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-1

Bit 7-3 **Reserved**: Maintain as '0b00000'

Bit 2-0 **SCLKOPT**: Sleep Clock Optimization

001: (default)

111: (optimized - Do Not Change)

LREG0x277: RFCTRL77

RF CONTROL 77							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
r	r	SLPSEL1	SLPSEL0	SLPVCTRL1	SLPVCTRL0	SLPVSEL1	SLPVSEL0
R-0	R-0	R/W-0	R/W-0	R/W-1	R/W1C-0	R/W-0	R/W-0

Bit 7-6 **Reserved**: Maintain as '0b00'

Bit 5-4 **SLPSEL[1:0]**: Sleep Mode Selection

00: (default) Standby mode

01: Deep sleep mode

10: Undefined

11: Power down mode

Bit 3-2 **SLPVCTRL[1:0]**: Sleep Voltage Control

11: Undefined

10: (default) Automatically controlled by internal circuit

01: Controlled by LREG0x277[1:0]

00: Undefined

Bit 1-0 **SLPVSEL**: Sleep Voltage Selection

00: (default - Do Not Change)

LREG0x27A: INITCNTL

INITIAL COUNTER LOW BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
INITCNT7	INITCNT6	INITCNT5	INITCNT4	INITCNT3	INITCNT2	INITCNT1	INITCNT0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **INITCNT[7:0]**: Initial Counter, Low Byte
User-defined initial counter for Upper Cipher operation. Only works when LREG0x24D[4] = '1'.

LREG0x27B: INITCNTH

INITIAL COUNTER HIGH BYTE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
INITCNT15	INITCNT14	INITCNT13	INITCNT12	INITCNT11	INITCNT10	INITCNT9	INITCNT8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-0 **INITCNT[15:8]**: Initial Counter, High Byte

Revision History

Revision	Date	Description of Change
0.0	2009/04/15	Generated from DS-2400-pre V1.5.
0.1	2009/07/14	Modify the description of the following sections and registers: 1) 3.4.2 Voltage Regulator 2) 3.5 Security Engine Block 3) 3.6.1 Crystal Oscillators 4) 4.2.5 Clock Recovery Time 5) 4.2.6 Sleep Mode Setting 6) 4.2.7 Change Channel Procedure 7) 4.5.1 Beacon Mode 8) 4.5.2 Beacon Mode GTS Setting 9) SREG0x2C SECCR0 10) LREG0x200 RFCTRL0 11) LREG0x22F TESTMODE 12) LREG0x23D GPIODIR 13) LREG0x206 RFCTRL6 14) LREG0x250 RFCTRL50
0.2	2009/08/17	1) 3.5. Security Engine Block: Remove description of Security suite of IEEE802.15.4-2003 2) 4.2.4 Initialization: Change optimized value of SREG0x3A to '0xBF' and re-arrange the sequence of SREG0x35. 3) 4.2.9. Turbo Mode Configuration: Add optimized setting of LREG0x206 and LREG0x207. 4) 4.4.2 Receive Packet with Security Decryption: Correct the procedure by adding Step 2. 5) 4.6 Power Saving Modes: Enhance operational procedure. 6) Appendix C: Re-write registers descriptions and correct POR values.
0.3	2009/11/05	1) 3.1.4 CCA: Enhance the description of ED mode 2) 3.2.5 CSMA/CA: correct the wrong description of SREG0x11[4:3] 3) 3.4.2 DC-DC Converter OFF Mode and DC-DC Converter ON/Bypass Mode: modify the setting for low voltage operation. 4) Restructure sections of chapter 4 5) 4.3.2 Clock Recovery Time: Add the descriptions of the WAKECNT setting of each power saving mode. 6) 4.3.6 Turbo Mode Configuration: Revise the setting of LREG0x206 for turbo mode 7) 4.4.3 Transmit Packet with Security Encryption: Rewrite. 8) 4.4.4 Transmit Packet in Normal FIFO with CCA/ED mode or combination of CS and ED mode: Newly added section. 9) 4.5.2 Receive Packet with Security Decryption: Rewrite. 10) 4.7.1 Wake-up Operations: Modify the procedures of 'Register Trigger'. 11) 4.9 Upper-Layer-Cipher Operations: Rewrite. 12) Appendix C: Revise the description of LREG0x24D[5].
0.4	2010/01/12	1) 3.4.2 DC-DC Converter OFF Mode and DC-DC Converter ON/Bypass Mode: rephrase the description. 2) Chapter 4 Application Guide: modify the bit names of LREG0x204[1:0], LREG0x22F[7], LREG0x274[7] and LREG0x274[3]

		3) Chapter 4 Application Guide: modify the Value on POR of LREG0x23D[5:4] 4) 4.3.1 Initialization: modify the description of LREG0x273 and LREG0x274 5) Appendix C: modify the default value of SREG0x34[5], bit name of LREG0x204[1:0] and LREG0x22F[7], description of LREG0x22F[6:3], LREG0x23D[7:4], LREG0x273[3:0], LREG0x274.
0.5	2010/03/10	1) 1.1 Device Pin Assignments: correct for SAW type package. 2) 3.7.4 Interrupt Signal: Modify the occasion of the generation of "WAKEIF" event. 3) 4.3.2 Initialization: add the setting of SREG0x3B and SREG0x3D. Modify the value of LREG0x202, LREG0x204, LREG0x206 and LREG0x207. 4) 4.7.2 Power Saving Operations: Rephrase description of "Power down mode" 5) Appendix C: Re-write registers descriptions of SREG0x3B, LREG0x202, LREG0x204 and LREG0x206. Add descriptions of SREG0x3D 6) 5.1 Package Drawing: Correct the drawing for SAW type package
0.6	2010/10/20	1) 2.2 Recommended Operating Conditions: Modify Note of table 3. 2) 2.3 DC Electrical Characteristics: Modify typical value of ACTIVE: TX and ACTIVE: RX. 3) 2.5 ESD Notice: Add CDM mode. 4) 3.1.4 CCA: Modify the description of "CS mode" and "ED mode". 5) 3.4.2 DC-DC Converter OFF Mode and DC-DC Converter ON/Bypass Mode: Modify the description and add Table 5, 6 and 7 for setting for different DC/DC modes. 6) 4.1 Hardware Connection: Modify figure 26. 7) 4.2.2 Register Summary: (and all the other register tables in Chapter 4) 7.1) Correct bit name of SREG0x1D[3], LREG0x200[1:0], LREG0x207[3:2], LREG0x220[6], LREG0x253[3:0], LREG0x259[0], LREG0x273[6] and LREG0x274. 7.2) Correct POR value of SREG0x22[6], LREG0x220[6], LREG0x223[1] and LREG0x23E[7:4]. 8) 4.3.1 Initialization: Modify the procedure and the setting value of LREG0x204, LREG0x207, LREG0x250 and LREG0x274. 9) 4.3.3 Change Channel Procedure: Modify description of step 3. 10) 4.3.6 Turbo mode configuration: Modify the value of LREG0x207 for 250k bps mode. 11) 4.4.1 Transmit Packet in Normal FIFO: Add note 2 to Step 1. 12) 4.4.2 Transmit Packet in GTS FIFO: Add note 2 to Step 1. 13) 4.4.4 Transmit Packet in Normal FIFO with CCA/ED mode or combination of CS and ED modes: Add Note 2 to Step 1. 14) 4.5.2 Receive Packet with Security Decryption: Correct the typo of Security Decryption Error bit in Step 8. 15) 4.6.1 Beacon Mode Setting: Add Note 2 to Step 4. 16) 5.2.2 Reference Reflow Temperature Curve: Modify Note to Pb-free SMD Package IR Reflow Profile. 17) Appendix A: Change to characteristic charts for Output Power and Sensitivity. 18) Appendix B TX Power Configuration: Modify the setting of LREG0x274. 19) Appendix C Register Descriptions: 19.1) Modify bit name of SREG0x1D[3], LREG0x200[1:0], LREG0x229[1:0], LREG0x253[3:0], LREG0x259[0] and LREG0x274[7:0]. 19.2) Modify optimized value of SREG0x3B[7:4], LREG0x204[1:0], LREG0x250[3:2]. 19.3) Modify Register type and POR value of SREG0x22[6] and LREG0x277[2]. 19.4) Modify register type of SREG0x28.

		19.5) Modify POR value of LREG0x223[1]. 19.6) Modify description of LREG0x202[7], LREG0x207[3:2], LREG0x253[5], LREG0x273[3:0] and LREG0x274[3:0].
0.6.1	2010/12/22	1) 2.3 DC Electrical Characteristics: Modify typical value of ACTIVE: TX, IDLE, HALT, STANDBY and DEEP SLEEP modes. 2) 3.4.2 DC-DC Converter OFF Mode and DC-DC Converter ON/Bypass Mode: Modify the setting for each DC-DC Converter Mode. 3) 4.3.1 Initialization: Modify the setting value of LREG0x201, LREG0x202, LREG0x206, LREG0x250, LREG0x273 and LREG0x274. 4) 4.3.6 Turbo Mode Configuration: Modify the setting value of LREG0x206 and LREG0x207. 5) Appendix A: Modify the characteristic curves for Output Power and Sensitivity.
0.6.2	2011/02/09	1) 4.1 Hardware Connection: Modify the reference circuit. 2) 4.2.2 Register Summary: (and all the other register tables in Chapter 4) 2.1) Correct bit name of LREG0x273[4]. 2.2) Correct register name of LREG0x220. 3) Appendix C Register Descriptions: 3.1) Modify the name of SREG0x1A and SREG0x3D in Summary Table of section C.1. 3.2) Modify optimized value of LREG0x250[3:0] and LREG0x273[7:6]. 3.3) Modify description of LREG0x273[4]. 3.4) Modify name of SREG0x1A[0] and LREG0x23C.
0.6.3	2011/09/01	1) 2.2 Recommended Operating Conditions: Modify Logical high/low input voltage. 2) Appendix C Register Descriptions: Modify optimized value of LREG0x206[5].

Contact UBEC:

Headquarters
Address: 6F-1, No. 192, Dongguang Rd., Hsinchu, 300 Taiwan
Tel: +886-3-5729898
Fax:+886-3-5718599
Website: http://www.ubec.com.tw

Sales Services
Tel: +886-3-5729898
Fax:+886-3-5718599
E-mail: sales@ubec.com.tw

FAE Services
Tel: +886-3-5729898
Fax: +886-3-5718599
E-mail: fae@ubec.com.tw

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